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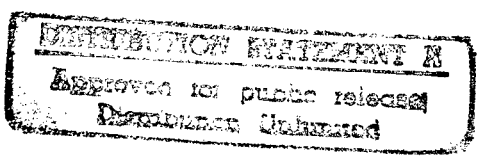

Science & Technology

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Goto Quantum Magneto-Flux Logic Project

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CONTENTS

[Final report of the Goto Quantum Magneto-Flux Logic Project (1 Oct 86 - 30 Sep 91), conducted as part of the Exploratory Research for Advanced Technology (ERATO) Project, administered by the Japan Research Development Corporation (JRDC)]

Goto Quantum Magneto-Flux Logic Project (1 Oct 86 - 30 Sep 91)

926C0009 Tokyo GOTO JISOKU RYOSHI JOHO PUROJEKUTO SAISHU HOKOKUKAI SHIRYO in Japanese 13 Sep 91 pp iii, 1-91

[Text]

Introduction

The Goto Quantum Magneto-Flux Logic Project, which was launched in October 1986, completed its 5-year term of research activities in September 1991. The Quantum Flux Parametron (QFP), first conceived in 1982, is a superconductive Josephson device that uses quantum flux as the logic unit. The characteristics of the QFP were analyzed through this project, and the QFP has been assessed to be a realistic device.

When a quantum flux is used as a logic unit, the device must always be operated in a superconductive state, and superb characteristics such as high speed and low power consumption are realized in comparison with conventional voltage-type Josephson devices. As part of the project, we performed a physical operation analysis of the QFP, and a basic circuit analysis of its computer system, making the most of its operational characteristics. We also conducted basic research on a generation of ultralow temperature/low magnetic field environment devices.

This report outlines the result of these studies, ranging widely from studies in physics, materials and devices of the magnetic flux to software. During these 5 years, the study of superconductive electronics has progressed rapidly, beginning with the discovery of high-temperature superconductive materials. We hope this project will be of use in preparing for the next widely expected step.

Meanwhile, superconductive research activities, which had been moving slowly following the retreat of IBM in the early 1980's, have now been revived. We have exchanged research results with the University of California, Berkeley, and the Massachusetts Institute of Technology, which boast of their high research levels, by conducting joint symposiums. It is expected that devices such as the QFP, which have a quantum flux as the logic unit, will find applications in forthcoming high-temperature superconductive materials. Through discussions at the symposiums, we felt strong expectations for the QFP thanks to its high speed and low power consumption.

We are hearing these days that Japan is getting a free ride in the area of basic research. This represents a new element of criticism against Japan. It is certainly true that not much research has been conceived in Japan and reared in the world. We sincerely hope that basic research themes launched under the creative scientific and technological promotion project will develop on a world scale, contributing to the realization of a richer human life in the future.

1. Description of the Project

(1) Purpose of the Quantum Flux Information Project

(i) Progress and Limit of Supercomputers

The supercomputer, which was invented in the mid-1960's, has increased its performance (see Figure 1) at the remarkable rate of about two-fold every year. Current models are capable of performing more than 1 billion operations per second. Along with this development, simulation technology, which makes it possible to replicate many phenomena by calculation on a computer, has been put into practice. From the aerodynamic design of cars and airplanes, and building design, through weather forecasting and nuclear furnace design down to super-LSI design and protein structure analysis, the number of areas where supercomputers are used keeps expanding, and supercomputers are now essential for research and development in virtually all scientific and technological fields. The reason for this is that the scale of the variables to be manipulated has become too large and massive to be tested with models designed on the basis of experience and intuition.

The operation circuit and memory circuit components of the current generation of supercomputers are composed of silicon LSIs. With development of super-LSI technology, in particular, downsizing technology has made it possible to produce elements smaller than 0.5 μm (0.5×10^{-3} mm), and this technology now enjoys a high degree of reliability thanks to the progress in packaging techniques for connecting these LSI chips.

However, it is assumed that a teraflops computer (capable of performing 1 trillion operations per second), which would be 100 to 1,000 times more powerful than the present generation of supercomputers, would be required to handle accurately more massive and complicated systems, such as long-term weather forecasting, typhoon course prediction, or precise structure analysis of genes and proteins.

It is generally believed that it will be impossible to realize this kind of ultra-supercomputer only through improvements to the current silicon technology. This is because cooling of the semiconductor circuit cannot catch up with the increasing exothermic density.

In other words, in addition to speeding up operations, it also is necessary to prevent signal delay by shortening the signal transmission distance, which in turn requires a smaller operation circuit.

When the signal transmission distance of an operation unit is assumed to be 30 cm or so per one-billionth of a second, it apparently is necessary to downsize the operation unit to a few square centimeters to have a supercomputer capable of operating 100 to 1,000 times faster than the present ones by shortening the machine cycle time. Since the calorific power per operation circuit realized with today's semiconductor technology does not

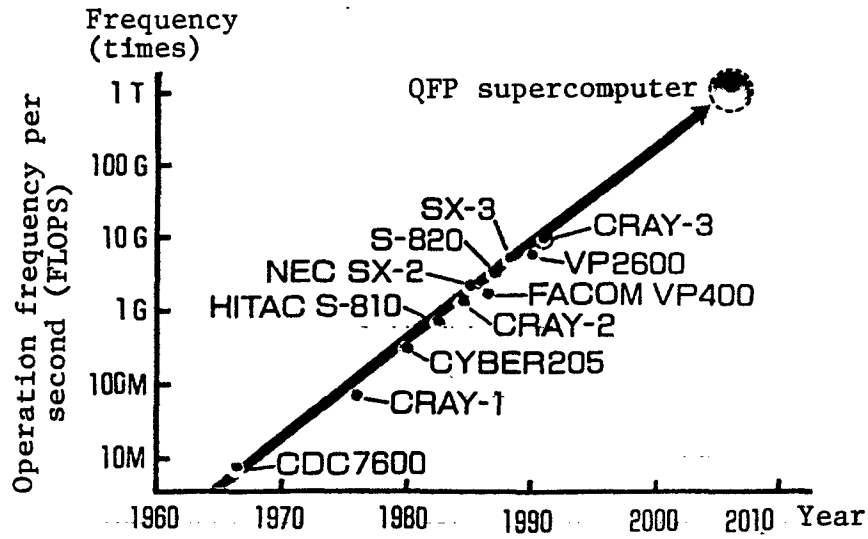

Figure 1. Progress of Supercomputers

change depending on the size of the device, the exothermic density of a downsized operation unit would be several kilowatts per square centimeter, which would be equivalent to the surface temperature of the sun. Considering that the maximum level of heat elimination that is currently possible is about 1 kW/cm^2, it is possible that an operation unit with such a high exothermic density could evaporate instantly. It is estimated that the limit of high density integration in silicon LSIs due to heating, or the limit of high-speed supercomputers will be reached by the end of this century or early next century. Therefore, to create an ultra-supercomputer with the capacity described above, it will be necessary to study devices featuring ultra-low power consumption and ultra-fast operational characteristics to replace conventional semiconductor devices.

(ii) Quantum Flux Parametron

The Quantum Flux Parametron (QFP) is a superconductive device announced by Professor Eiichi Goto, the leader of the project, in 1983.[1] As its basic operation is similar to the Parametron Device[2] (also invented by Professor Goto in 1954), which consists of a ferrite core, a coil, and a condenser, the former was named using the term "parametron"—a genuine domestic logical device product. A schematic diagram of its circuit configuration and a corresponding cross section diagram are shown in Figure 2. The QFP consists of two superconductive loops, two Josephson junctions, and an inductance line. When a current flows to the excitation line in synchronization with the input, a flux quantum is trapped in one of the loops depending on the input signal. By designating one of them as "1" and the other "0," a digital logic circuit can be structured. This is a high-performance device having the three essential functions—memory, operation, and amplification—required for computer devices.

As the quantum flux is used as a logic core, the QFP has two important features—high speed and low power consumption.

A conventional semiconductor device and the superconductive device are compared in Figure 3 in terms of their power consumption and delay time. For the semiconductor device, MOS, bipolar (silicon), and MESFET (compound) types were used, while for the superconductive device a typical Josephson device and QFP were used for comparison. As can be seen from Figure 3, the power consumption of the QFP is 1 million times less than that of a bipolar semiconductor device, and 1,000 times less than that of a typical Josephson device. Furthermore, the QFP operates at the ultrahigh speed of one-trillionth of a second—10 times faster than the fastest semiconductor device of today.

The third feature of the QFP involves its magnetic flux junction characteristics. It features signal transmission without electrical contact. This is possible because the magnetic flux is the logic unit for a QFP. Therefore, as shown schematically in Figure 4, it is possible to achieve three-dimensional connections simply by stacking chips to produce more compact system configurations. This leads eventually to an ultrahigh density packaging of the operational unit required for an ultrahigh-speed supercomputer.

Because of these excellent features—ultrahigh-speed switching, low power consumption, and three-dimensional packaging by magnetic flux junction—the QFP has great potential as a device for use in the ultrahigh-speed supercomputer of the future.

(iii) Purposes of the Project

The purposes of the Goto Quantum Magneto-Flux Logic Project, which was organized against this background, can be summarized as follows:

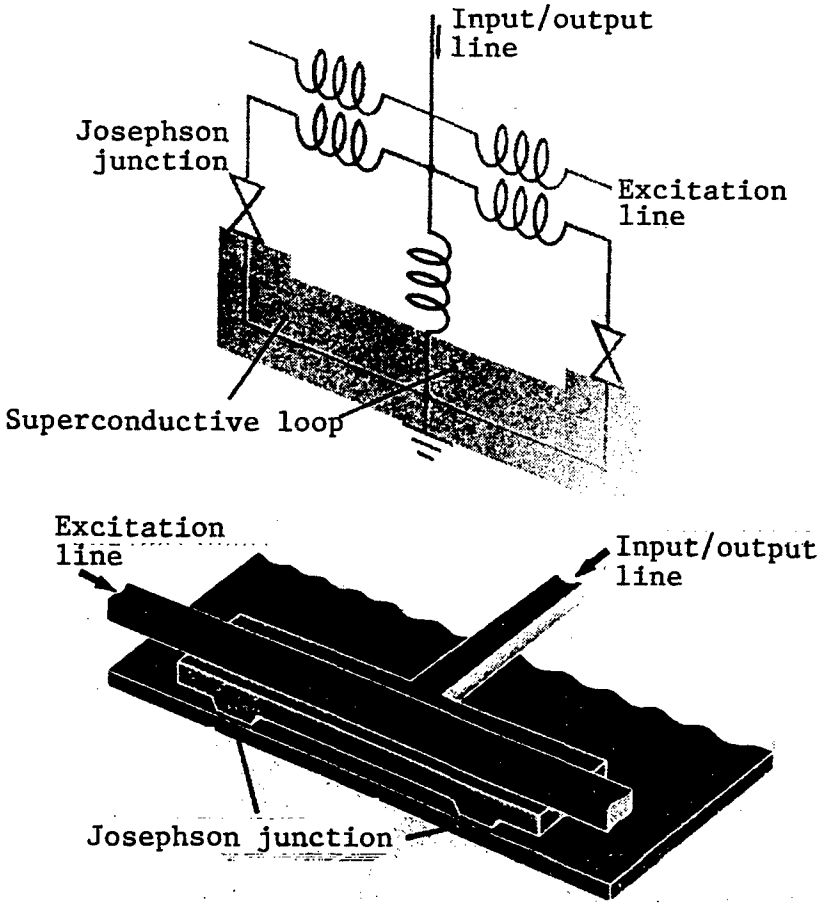

Figure 2. Schematic Circuit and Cross-Section Diagrams of Quantum Flux Parametron (QFP)

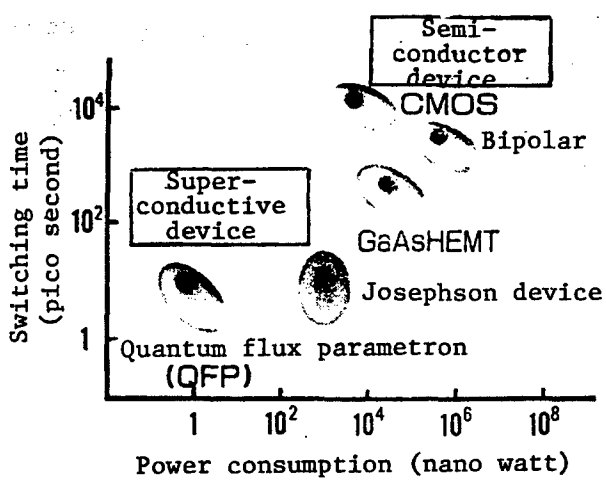

Figure 3. Comparison of Devices for Switching Time and Power Consumption

The first purpose was to assess whether the characteristics of the QFP are such that it could serve as the basic device for future ultrahigh-speed supercomputers. This involves studying its characteristics in terms of suitability as an ultrahigh-speed supercomputer device by developing appropriate evaluation techniques. This includes measuring the basic operational characteristics of the QFP; studying the substrate technique, including such circuit designs as three-dimensional inductance computation; examining the ultrahigh-speed movement and high performance QFP logic circuit; and verifying circuit operations based on the three-dimensional packaging technique.

Second, the project has proposed the cyclic pipeline architecture (CPA) as a computer system appropriate for these operational characteristics. In part, this is because the QFP itself has a latch function for storing data, which is different from the past semiconductor or voltage-output type superconductive devices. The project also was aimed at designing and manufacturing a computer based on CPA using silicon IC's to examine the true effectiveness of the CPA.

Third, the project sought to explore high-performance and highly reliable refrigerator and magnet-shielding

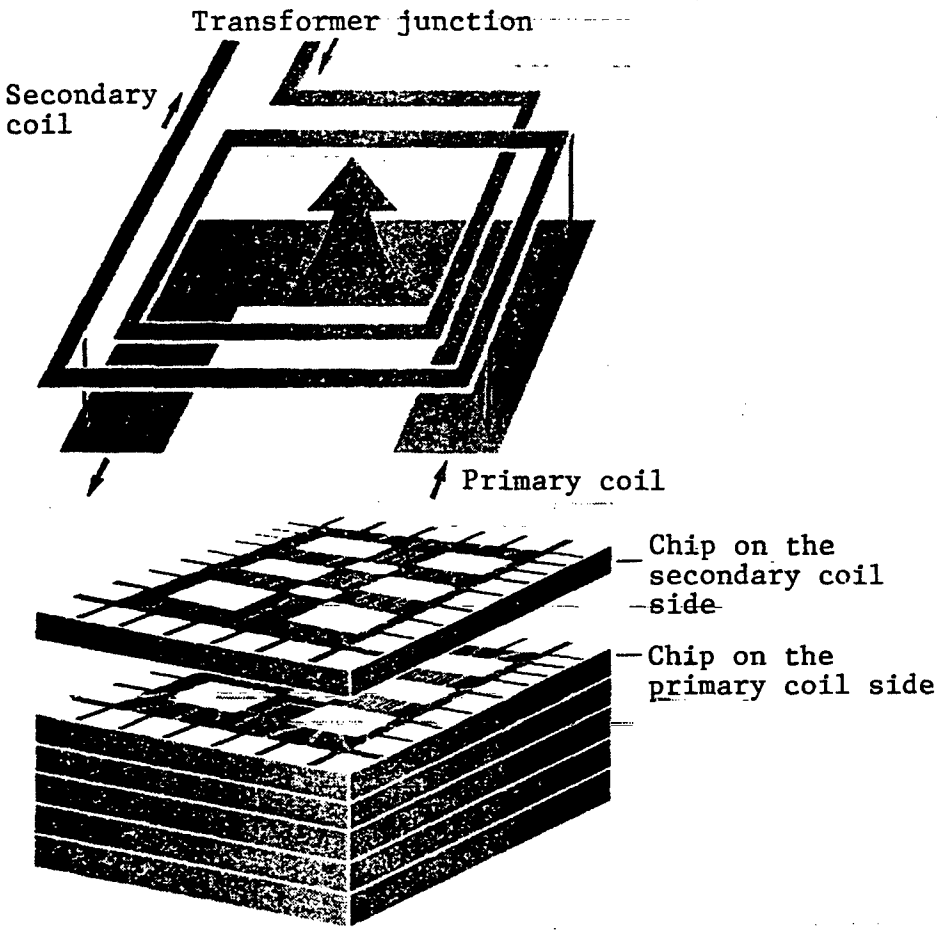

Figure 4. Conceptual Diagram of Three-Dimensional Packaging

technology. Such technology is essential because the QFP operates with the magnetic flux as the logic unit in a superconductive environment, which requires an ultralow temperature of absolute 4.2°K and an ultralow magnetic field about one-millionth that of the earth.

To meet these study requirements, the project organized three study groups.

(2) Study Organization and Main Research Themes

The study organization of the Goto Quantum Magneto-Flux Logic Project consisted of three study groups. The location, main research themes, and group leader (original office) for each group, together with the duration of the study, are shown below:

(i) Fundamental Property Group: Central Laboratory, Hitachi, Ltd.

Study items: Physical and operational characteristics of QFP devices; Physics of device operations, logic circuit system, high-speed operation circuit system, packaging system, other application circuits, physical limit of devices, device design system

Group leader: Yutaka Harada (Central Laboratory, Hitachi, Ltd.) (October 1986-March 1989); Ryotaro Kamikawai (Central Laboratory, Hitachi, Ltd.) (March 1989-September 1991)

(ii) Magnetic Shielding Group: Mitsui Shipbuilding Company, Ltd. (October 1986-September 1990); Central Laboratory, Hitachi, Ltd. (October 1990-March 1991)

Study items: Ultrahigh-speed computer architecture (Cyclic Pipeline Architecture (CPA)), experimental verification of CPA, application software

Group leader: Norihiro Fukazawa (Mitsui Shipbuilding Company, Ltd.) (October 1986-September 1990); Mitsuhisa Sato (Tokyo University) (October 1990-March 1991); Ikuo Wada (Central Laboratory, Hitachi, Ltd.) (March 1991-September 1991)

(iii) Computer Architecture Group: Japan Vacuum Technology Company, Ltd.

Study items: Ultralow temperature and ultralow magnetic field environment creation technology; Detection and removal of trapped magnetic flux (micro heat flush method), high-performance refrigerator system, high vacuum technology

Group leader: Junpei Yuyama (Japan Vacuum Technology Company, Ltd.) (October 1986-September 1991)

(3) Participants

Table 1 shows the participants in this project, the duration of their studies, the main research themes, and the original office name. A total of 21 people participated as researchers, with 10 from five corporations mainly at the study location, six individual researchers who had just graduated from college, and five foreigners (one each from the Netherlands, Spain, China and two from Singapore) following their graduation from overseas colleges, including postdoctorates. There was a total of 11 doctorate holders, including six who obtained the title during this project. Also, five foreign researchers from three countries (the United States, England and Singapore) participated on a short-term basis. In addition to these, five engineers participated on both a long- and short-term basis.

Table 1. Researchers Who Participated in This Project and Their Study Themes

Fundamental Property Group	
R. Kamikawai (Hitachi, Ltd.)	High-speed excitation system, three-dimensional packaging system
S. Shimizu (Seiko Electric Industry Company, Ltd.)	Analysis and verification of device's fundamental operations
H. Nakane (Hitachi, Ltd.)	Circuit creation process, low-noise flux parameter
Y. Harada (Hitachi, Ltd.)	Analysis and verification of device's fundamental operations, high-speed analog-to-digital conversion
N. Miyamoto (Hitachi, Ltd.)	Circuit creation process
I. Wada (Hitachi, Ltd.)	Device downsizing rule and physical limit
R. Suda (Tokyo University)	High-function logical circuit system
J. Casas (Lausanne University)	Verification of speed operation, low-noise flux parametron
W. Hioe (Singapore National University)	High-function logical circuit system, device physics
Magnetic Shielding Group	
J. Yuyama (Japan Vacuum Technology Company, Ltd.)	New-type pulse-tube refrigerator
M. Kasuya (Alpack Cryo Company, Ltd.)	New-type pulse-tube refrigerator, ultra vacuum cryopump, electro-deposited nickel film fatigue strength
K. Chihara (Hokkaido University)	Reduction of bellows stress by multilayering
H. Minami (Kumamoto University)	Detecting and sweeping flux quanta trapped in superconductors
Q. Geng (Copenhagen University)	Detecting and sweeping flux quanta trapped in superconductors
Computer Architecture Group	
M. Sato (Tokyo University)	Cyclic pipeline architecture, FLATS FORTRAN compiler
N. Fukazawa (Mitsui Shipbuilding Company, Ltd.)	Development of FLATS2 system software
S. Ichikawa (Tokyo University)	Design of FLATS hardware
S. Kawakami (Mitsui Shipbuilding Company, Ltd.)	Evaluation of FLATS2 arithmetic instruction
P. Spee (Delft Engineering University)	FLATS2 C compiler, implementation of CPX operation system kernel
W. F. Wong (Singapore National University)	Fast elementary function algorithm, computer capacity evaluation system

The project has enjoyed guidance and instruction from the following individuals who served as study advisors and study promotion members.

Study Advisor:

K. Kamata	Executive director, Nishina Memorial Foundation

Study Promotion Members:

T. Otsuka	Chief engineer, Technical Development Division, Japan Vacuum Technology Company, Ltd.
T. Ogata	Chief researcher, Metallic Materials Laboratory, Science and Technology Agency
Y. Koyanagi	Professor, Information Science Department, Faculty of Science, Tokyo University
T. Kobayashi	Professor, Physics Department, Faculty of Science, Tokyo University
S. Kawabe	Chief researcher, Central Laboratory, Hitachi, Ltd.
M. Suzuki	Researcher, Information Science Laboratory, Riken Institute
T. Soma	Chief, Computer Room, Riken Institute
F. Naruse	Chief engineer, Technological Development Division, Japan Vacuum Technology Company, Ltd.
K. Nakazawa	Professor, Electronics Information Engineering Division, Tsukuba University
T. Nakano	President, Japan Address Type Company, Ltd.
Y. Miki	Chief researcher, Measurement Laboratory, Industrial Technology Agency, MITI
Y. Yoshida	Researcher, Goto Special Laboratory, Riken Institute
A. Yonezawa	Professor, Information Science Department, Faculty of Science, Tokyo University

The following members also were invited to serve as guest researchers for study and guidance.

Prof. Loe Kia Fock	Department of Information Science, National University of Singapore
Dr. Jonathan B. Green	Lincoln Laboratory, Massachusetts Institute of Technology
Prof. Roger W. Hockney	Professor Emeritus, University of Reading
Dr. Emerson Fang	Department of Electrical Engineering, University of California, Berkeley
Dr. Peter P. T. Tang	Mathematics and Computer Science Division, Argonne National Laboratory

(4) Study Progress and Results

This section describes the progress and principal results of each study group. Details are given in Chapter 3, which presents the reports of each researcher, but a summary is given here in terms of the time-based progress and study items of each study group. The 5-year duration of the project was not necessarily smooth, and the following is focused only on those studies that produced some final results.

(i) Fundamental Property Group

The Fundamental Property Group first studied the operational principles and physical phenomena of QFP. The group also studied such fundamental tasks as the evaluation techniques to ensure accurate measurement of QFP device characteristics, and the support technology for QFP circuit designs. It thereby established infrastructure technology, such as the minimal signal measurement technique with a SQUID and the three-dimensional inductance simulation technology. The group devoted half of the total project to these studies.

Next, the group concentrated on studies of the high-function logical circuit designs, and succeeded in proposing and verifying a stable, high-function logic circuit.

As this circuit can be compared to the transistor-to-transistor logic (TTL) circuit, the group named this circuit QFP-to-QFP logic (QQL). Figure 5 shows its basic circuit and the configuration of the elements.

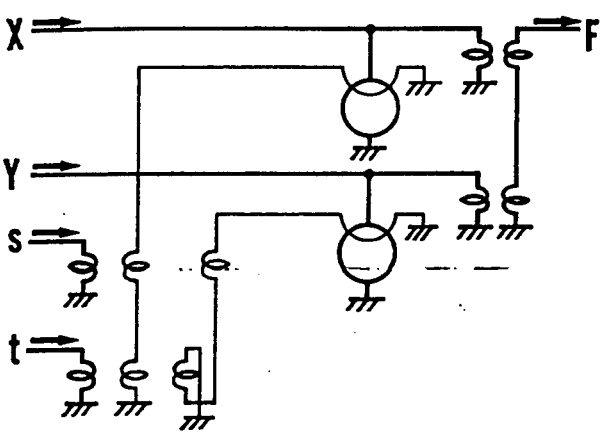

Figure 5. Basic Circuit of D-GATE

We named this circuit "D-GATE" after its functions. Conventional systems have used a so-called "wired logic" system that inputs the signal directly to the QFP's input transformer. The D-GATE circuit, however, uses a composite logic system that drives the next-stage QFP with a QFP. This makes it possible for a high-function logic circuit to have the following function for the four inputs of s, t, x, and y:

$$z\,(x, y, s, t) = x\,(s = t) + y\,(s \text{ not equal to } t)$$

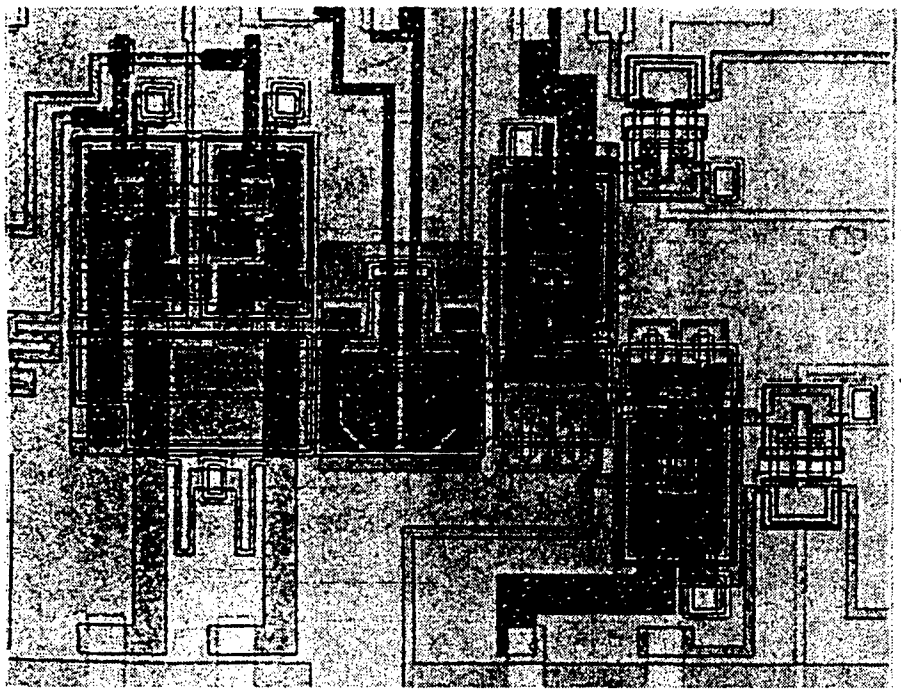

Figure 6. Microphotograph of D-GATE

A microphotograph of the test-produced circuit is shown in Figure 6.

From this circuit operation, the logic function has been verified. In parallel with this study, the group has established a logic design system using D-GATE. They have designed the basic logic circuit, such as a full adder and multiplier, and have demonstrated that it is possible to design circuits having similar functions but with far fewer elements than conventional semiconductor circuits. For example, its full adder has only two D-GATEs and about 20 4-bit multipliers. This is about one-fourth of the elements found in semiconductor devices.

For the two most significant features of QFP—ultrahigh-speed operation and low power consumption—it was impossible to verify the low power consumption in practice and they had to be satisfied with a logical computation. The reason for this is that since the power consumption per logic gate is as little as one-billionth of a watt, it is necessary to operate at least several million devices at a time to measure the caloric value accurately with current techniques. This, however, falls outside the purpose of this project, and also lies beyond the capabilities of current technology. Meanwhile, to verify the ultrahigh-speed operation characteristics, they used a shift register, which transfers sequentially one element per clock of the digital data as shown in Figure 7. To make it possible to evaluate the high-speed operation characteristics, a highly accurate measurement technique for the circuit operation characteristics was established by improving the low-noise measurement technique.

With this low-noise accuracy measurement technique, it became possible to verify that even a 5-μm device is capable of a high-speed operation equivalent to 15 ps (1 ps: one-trillionth of a second) at 16 GHz (1 GHz: 1 billion times per second) and four-phase excitation as shown in Figure 8.

This speed is possible only with a semiconductor device using an ultraminiature processing technology of less than 0.5 μm, and the high-speed capability of QFP was thus verified.

Furthermore, this study of the high-speed operational characteristics demonstrated that the operational characteristics of QFP agree closely with the simulation, which made it easier to forecast these characteristics in subsequent studies.

For a minimum processed size of 2.5 μm, a simulation verified a performance level of 100 GHz, but, due to the limitations of the measurement instrument, only an ultrahigh-speed operation of about 40 GHz could be tested. Using a so-called submicron technology of less than 1 μm minimum, it became possible to operate at speeds as high as 1 THz (1 trillion times per second) through a theoretical study.

By improving the low-noise accuracy measurement further, a real-time measurement of the QFP operational characteristics at 5 GHz (which formerly was believed to be impossible) was realized as shown in Figure 9. This

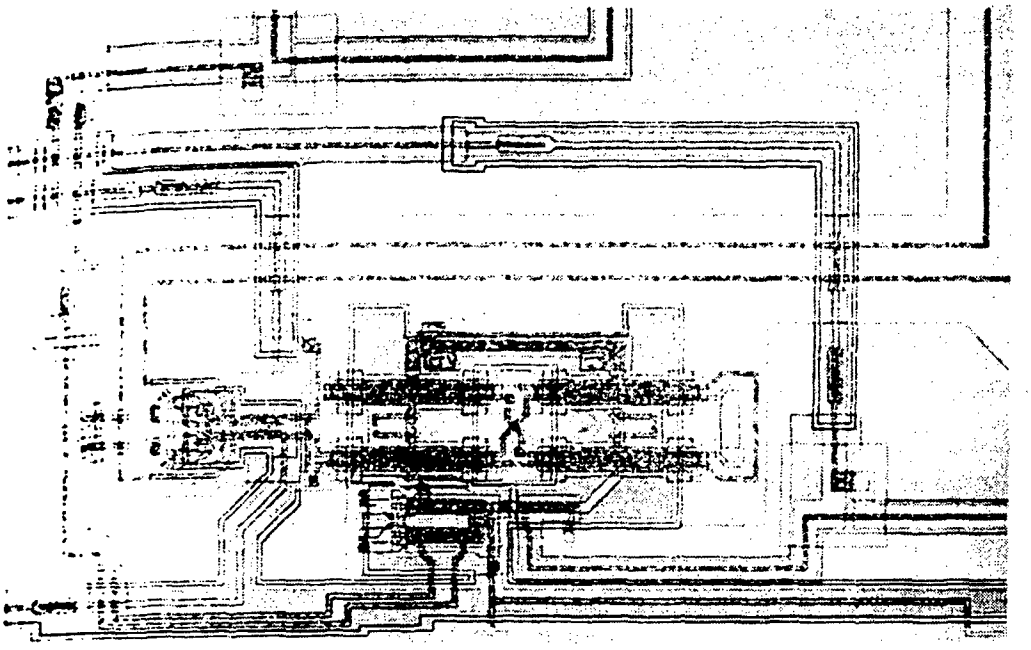

Figure 7. Shift Register Used in Measuring High-Speed Operation Characteristics

technique is designed to detect a minimal signal of less than 10 μV (1 μV: one-millionth of a volt) and amplify it while reducing noise.

Compared to conventional semiconductor technology, it became possible to take out in real time a minimal signal about 10,000 times less powerful.

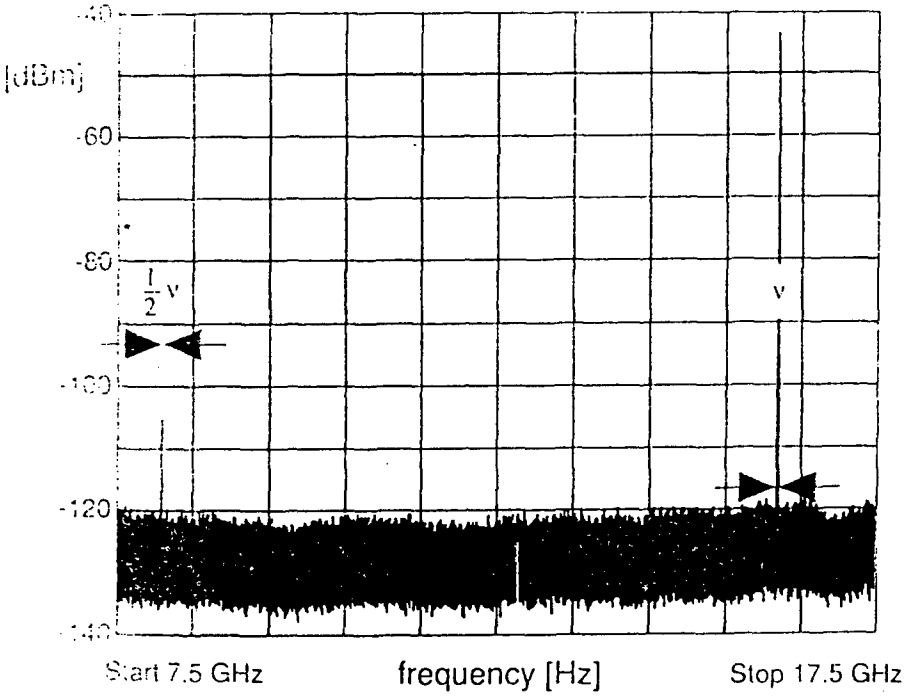

Figure 8. 16-GHz Operation Characteristics of the Shift Register Circuit

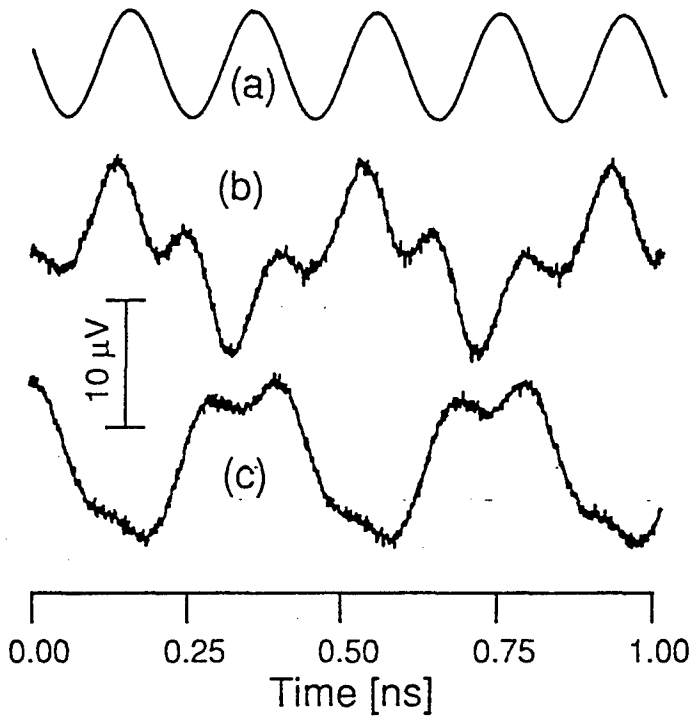

Figure 9. Results of Real-Time Measurement of QFP Operational Characteristics (Data at 2 GHz)

The waveform of this operation also agrees with the simulation, which confirms that operation of the QFP device is consistent with analytic predictions.

We said before that it is possible to transmit signals by a flux junction, and the QFP is a quantum flux device. Thus, the group studied a new three-dimensional packaging method to make the most of this feature. This three-dimensional packaging method is based on signal transmission through transformer junction only. This is accomplished by stacking the chips that incorporate the QFP circuit. With ordinary semiconductor devices, signal transmission is effected by connecting metallic terminals directly, but metallic terminals create problems in terms of reliability and high-density packaging, among others. With the transformer junction, these problems can be solved since compactness and high reliability are easier to achieve.

The group determined the transformer and other constants between two chips, which are important for the three-dimensional packaging device design, using three-dimensional inductance simulation technology. Further, during the design process, it became clear that the positioning of the upper and lower chips is an important parameter that affects the signal transmission characteristics. Thus the group designed a new, accurate positioning unit for three-dimensional packaging, as shown in Figure 10, and used the test-manufactured unit for experiments in stacking two chips, as shown in Figure 11.

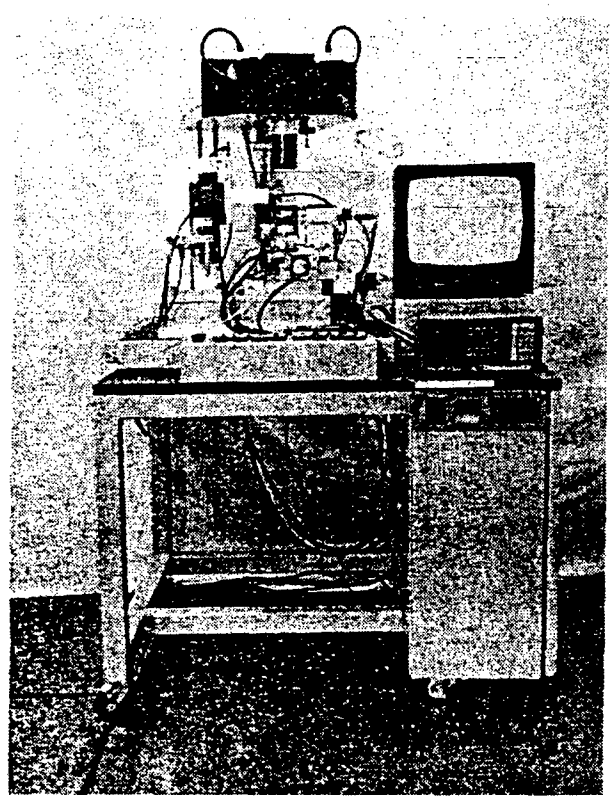

Figure 10. Accurate Positioning Unit for Three-Dimensional Packaging

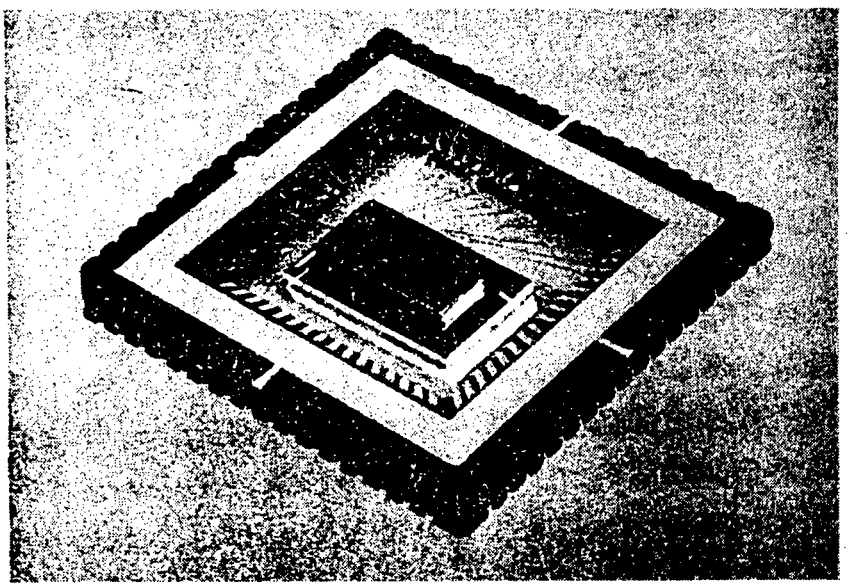

Figure 11. Photo of a Chip With Three-Dimensional Packaging

As shown in Figure 12, the group verified signal transmission from one chip to another via the flux junction, and succeeded in clarifying its characteristics.

The QFP can be used for applications involving high-speed analog-to-digital (A/D) conversion, in addition to digital operations. By checking its high-speed operational characteristics, we learned that it is possible to process input signals at a sample frequency of 18 GHz, even with a processed size of 5 μm. When the processed size of the device is further reduced, an ultrahigh-speed A/D converter that can operate at a few dozen GHz becomes possible.

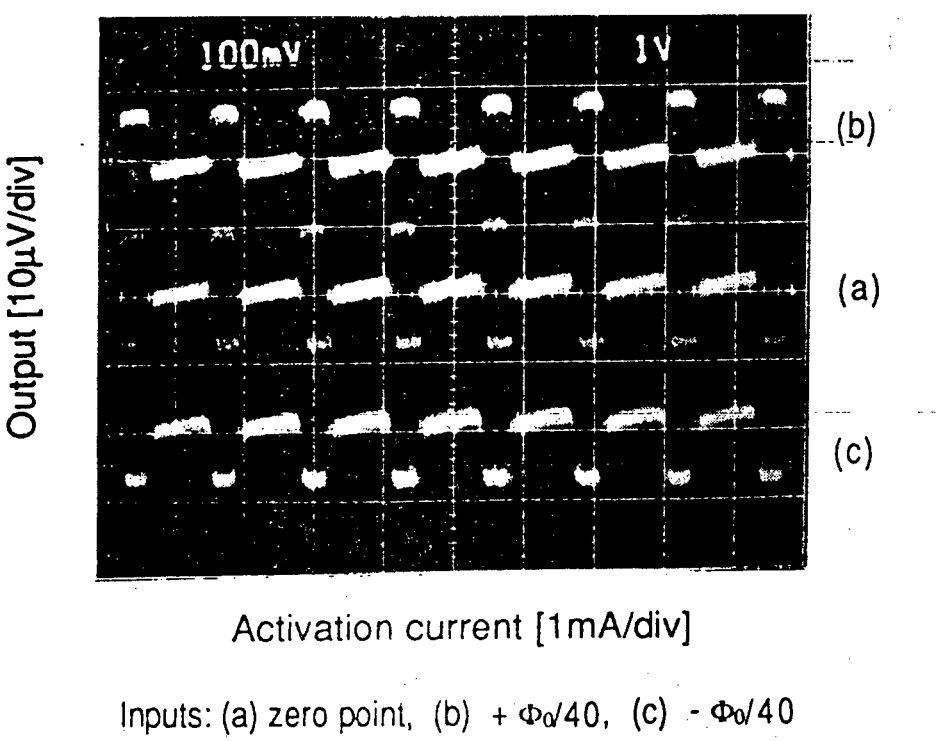

Figure 12. Noncontact Signal Transmission Characteristics of a Chip With Three-Dimensional Packaging

As the results of this study demonstrate, the QFP is capable of achieving high speed and high performance by downsizing the processed size. Therefore, the group discussed the proportional downsizing rule for QFP, together with its physical limits, and came up with a prospect for the future. The physical limits of the QFP are determined by the invasion length of the flux into the superconductors, and the minimum size would be about 0.1 μm. Further, from the viewpoint of heating, the integration limit would be about 0.04 μm minimum for the processed size. Meanwhile, since the QFP uses the quantum flux as a logic unit, malfunctions due to heat noise and the quantum tunnel phenomenon may occur. This is because its energy consumption is so low in spite of its high speed, as shown in Figure 13.

From these physical limits and the proportional downsizing rule, it was possible to clarify the minimum processing size, and the limits of power consumption and delay time. Further, we demonstrated that it is possible to realize a QFP supercomputer with a minimum processing size of 0.25 μm on a 1 cm^2 chip, even using a high-temperature superconductor.

Because the QFP device uses an inductance load, there are some limits in its design. For example, the length of the input wiring and the inductance balance between several outputs must be optimized. Therefore, the group tried to obtain design guidelines by analyzing the limiting items quantitatively. As a result of detailed analysis, the maximum value of QFP output inductance, and the limit of the allowable range were clarified quantitatively in order to obtain design rules for the forthcoming massive integration of circuit design.

Further, the group studied the structure of a highly sensitive fluxmeter, although this was not directly related to the study of the QFP. By providing an ordinary SQUID fluxmeter with negative inductance, it was demonstrated both analytically and experimentally that device noise could be reduced to about one-tenth.

Further, the group discussed the information logic. As a result of studying the QFP's operational characteristics in detail. We learned that, when the QFP operates at as low a speed as possible, its energy consumption could be reduced indefinitely. A so-called noncalorific energy computation principle, that is, no energy is consumed in generating or eliminating information, was clarified. Conventional information theory assumes that an amount of energy W = k 1 n 2 is generated or disappears along with generation or disappearance of 1 bit of information. However, we learned that this theory is based on an incorrect application of thermodynamic entropy for information entropy.

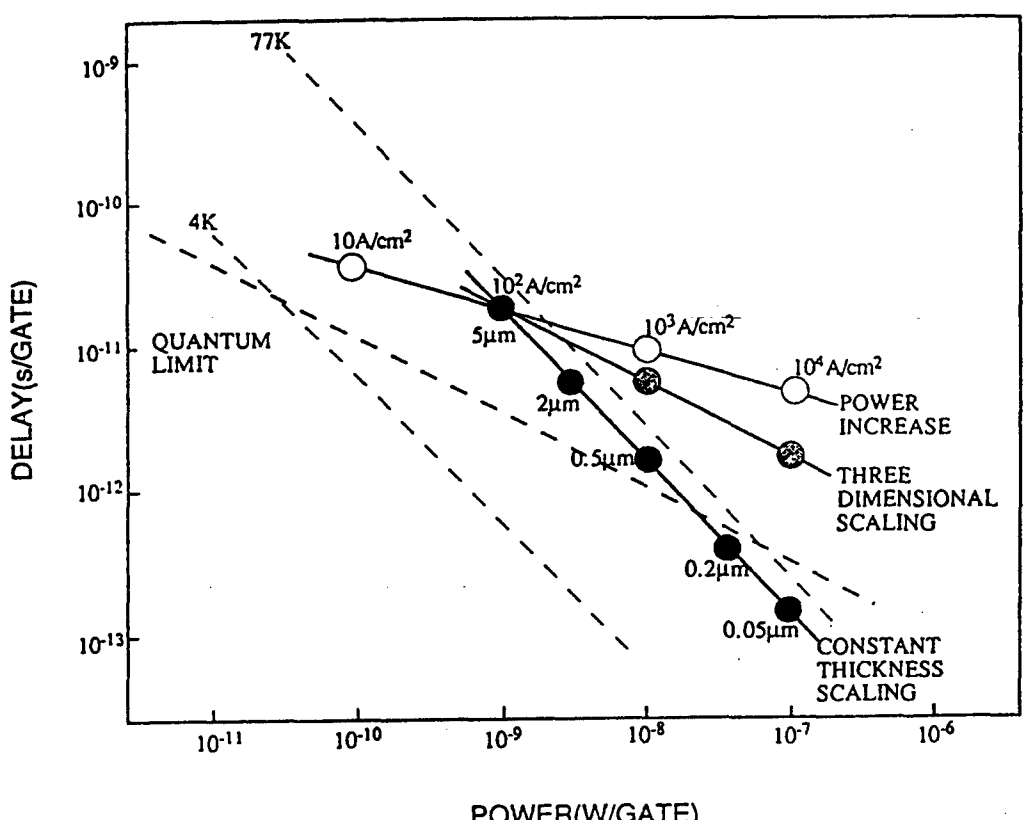

Figure 13. Proportional Downsizing Rule and Physical Limits of QFP

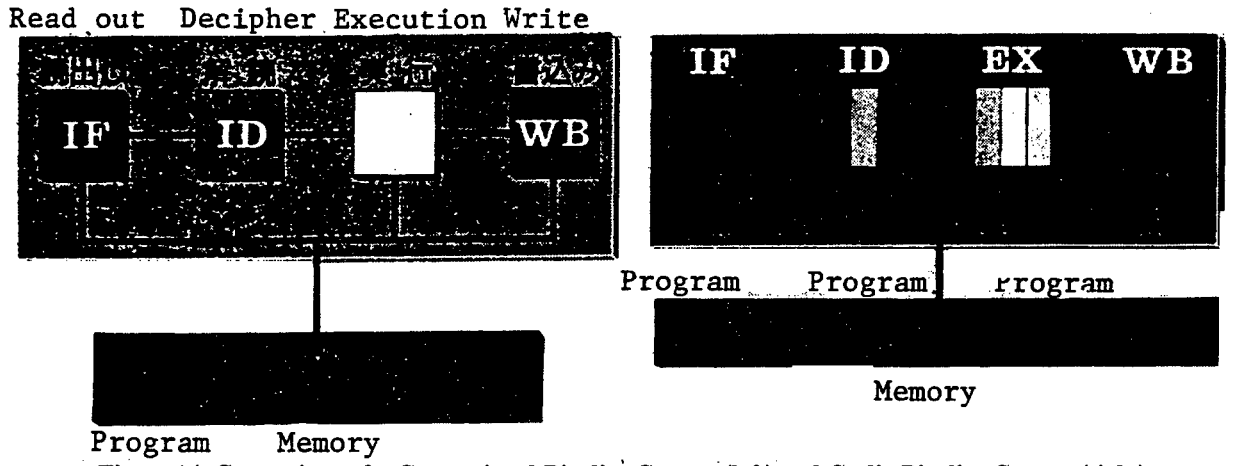

Figure 14. Comparison of a Conventional Pipeline System (left) and Cyclic Pipeline System (right)

(ii) Computer Architecture Group

The Computer Architecture Group sought primarily to verify the effectiveness of the Cyclic Pipeline Architecture (CPC). The CPC is a computer architecture that is appropriate for devices such as QFP, which operates at a high speed by latching information for every clock. As shown in Figure 14, this architecture segments pipelines more minutely per stage than conventional pipeline architectures, and feeds information sequentially into these pipelines while running several programs.

When a computation is executed using the results of the preceding computation, with the past method it is necessary to wait for the results of the preceding computation, and computation is suspended during such time. The cyclic pipeline architecture, however, feeds information for different programs into pipelines sequentially, thus wasting less time and assuring higher performance from similar hardware.

Therefore, this architecture is suitable for a device such as the QFP, whose operational characteristics are such that it latches data at ultrahigh speeds. This architecture is useful not only for the QFP, but also for devices having a latch function. For example, it is suitable for a latch device using a silicon semiconductor. Therefore, it has a promising future as an architecture for ultrahigh-speed computers.

In this project, the group created the cyclic pipeline architecture's system kernel (CPX) and compilers using the FORTRAN and C languages. Further various application programs also were prepared. A simulation using this software confirmed the effectiveness of CPC.

In parallel with this, the group manufactured a CPC computer (FLATS2) based the cyclic pipeline architecture shown in Figure 15 using a silicon IC. It was designed using standard logic IC's (ECL10K, 100K, etc.). This was a difficult study that required about 3 years

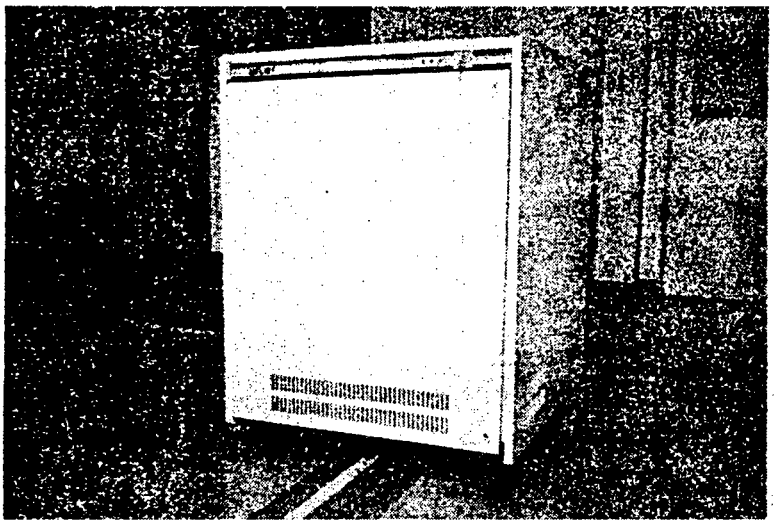

Figure 15. Cyclic Pipeline Computer FLATS2 Test-Manufactured Using Silicon ECL IC

from the start of its logic design to completion of the test. Because it used a standard logic IC, there were some problems, such as high calorific value (power consumption), and complicated and extensive wirings between boards, which required some novel techniques, especially in packaging. The FLATS2 is assumed to be a parallel computer with two operation units, and it has achieved a high performance level—this was expected to be about 1.8 times higher than with one operation unit—as demonstrated by the benchmark test shown in Figure 16.

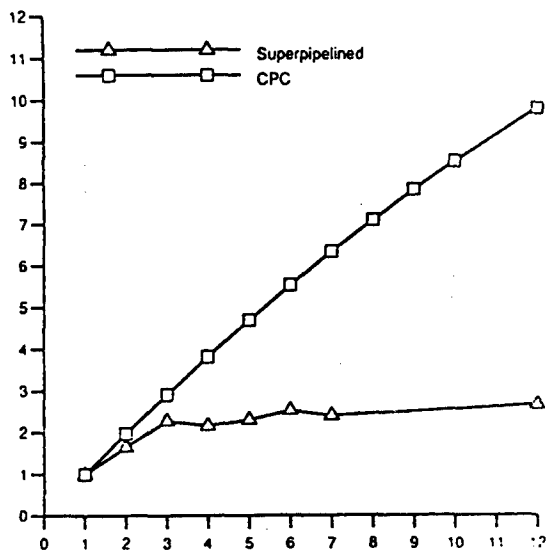

Figure 16. Comparison of Efficiency Between the Cyclic Pipeline System (square) and Conventional Pipeline system (Δ)

The simulation served to confirm that a CPC computer with 12 operation units is capable of performing about 10 times higher than is possible with one unit. Under similar conditions, the conventional pipeline architecture can improve performance only by two to three times.

In this way, the excellent features of the cyclic pipeline architecture, as compared to ordinary pipeline architecture, was confirmed.

It is known that, although it is possible to achieve a performance level on the order of a score of GFLOPS for an ultrahigh-speed computer using QFP, several special techniques are required to realize a performance level of 1TFLOPS in practice. Therefore, the group studied the prospect of developing 1TFLOPS ultrahigh-speed supercomputers. As the time for conducting the study was limited, the group dealt only with the high-speed elementary function algorithm, an ultrahigh-speed computer evaluation method, and a cyclic pipeline multiprocessor during the project period. One possibility for attaining this performance level was obtained by operating 16 to 64 10-GHz CPC processors in parallel.

(iii) Magnetic Shielding Group

Because the QFP uses quantum flux as the logic unit, its operation requires an ultralow temperature and magnetic field environment. Therefore, the environment control group studied highly reliable and highly efficient refrigerator and nonmagnetic field creation technology. Since currently it is possible to have a Josephson junction with good repeatability only through the use of low-temperature superconductivity technology using niobium metal among others, the group explored the possibilities of creating a highly reliable liquid helium refrigerator. As the QFP operates with one quantum flux as its logic unit, it is vital that the external magnetic field be minimized, and, at the same time, it is possible that the QFP may malfunction due to the influence of the flux trapped in the superconductor. Therefore, this group studied techniques for removing fluxes trapped in superconductors. To realize a highly reliable and highly efficient liquid helium refrigerator, the group first studied a refrigerator with a bellows for the compressor pump section.

Because it was assumed that the weakest point of the bellows, which functions as the helium compressor, lies in its fatigue strength, laminated materials of high and low Young's modulus were used in a simulation based on the finite element method to assess their stress distribution.

As a result, we learned that maximum stress can be reduced when materials where the Young's modulus varies by a factor of 100 are laminated. In parallel with this study, the group obtained the fatigue strength of nickel electro-deposited films by experimentation. This measurement was made by counting the number of vibrations produced when a cylindrical material is vibrated repeatedly at a frequency of tens of herz until it breaks down. As a result, the fatigue strength of nickel electro-deposited films was clarified.

Because a bellows-type refrigerator is limited by the physical properties of its materials, the group studied a new type of pulse tube refrigerator that absorbs work by providing a piston at the room-temperature terminal.

As this new type of refrigerator has no moving parts in its low-temperature section, highly reliable operations can be expected.

Inserting an orifice to maintain the shape and laminar flow of the pulse tube made it possible to verify its high cooling capability and its high reliability.

To create a more capable refrigerator, it is necessary to have a design technology that incorporates many simulation techniques, such as obtaining the exact solution of the Navia-Stokes formula using a supercomputer, and that is not satisfied with conventional design techniques that are based on experience only.

As the QFP uses the quantum flux as its logic unit, its operational characteristics are subject not only to the external magnetic field, but also to the quantum flux trapped in the superconductive film. Therefore, the group studied ways to establish a micro heat flush technique for removing the flux trapped in the superconductive film.

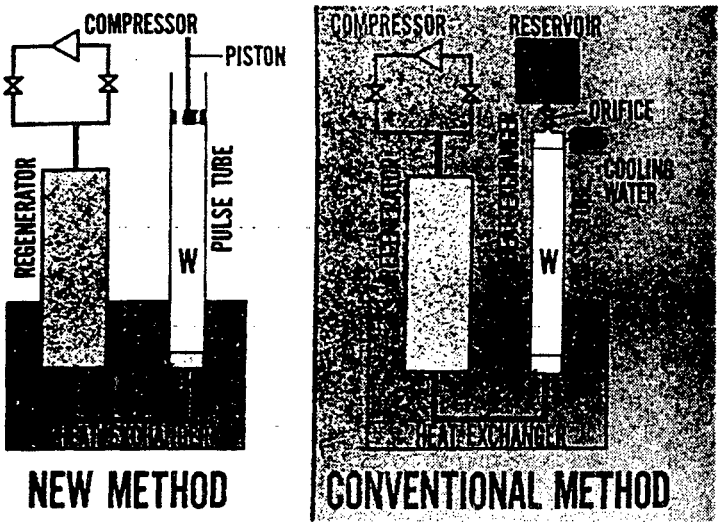

Figure 17. Comparison of Structures of New-Type Pulse Tube Refrigerator (left) and Conventional Refrigerator (right)

This micro heat flush method involves detecting the position of the quantum flux trapped in a superconductive film with a SQUID, locally heating its periphery with a laser beam to make the superconductive film conductive in a normal way, shifting the flux, and removing the flux from the superconductive film. This process is shown in the diagram of Figure 18.

To keep the distance between the superconductive film and the SQUID's pickup coil constant, a gas floating head based on Bernoulli's theorem was conceived. The SQUID can detect the trapped flux with a flux resolution of 0.1 Φ_o, and a position resolution of about 100 μm (about one-tenth of the pickup coil diameter).

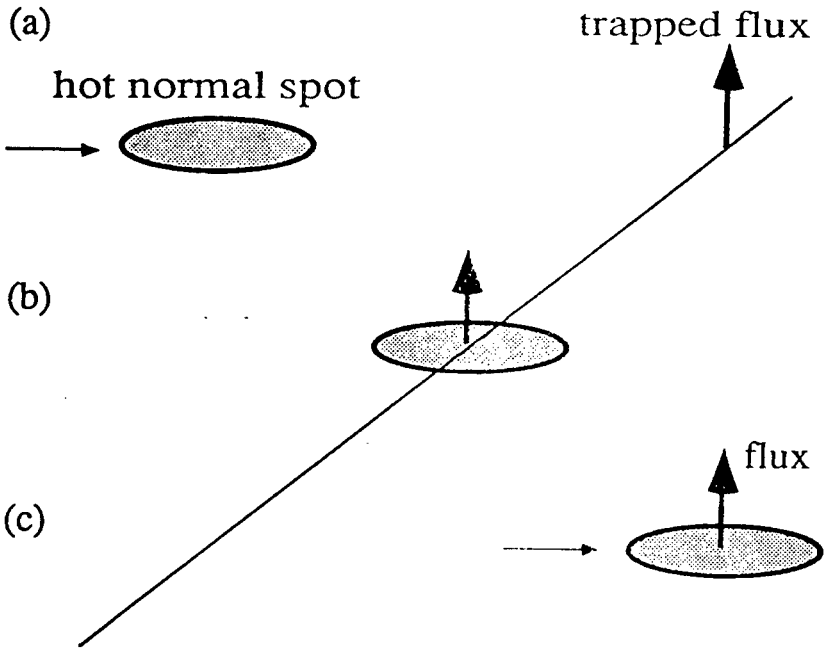

Figure 18. Principle of Micro Heat Flush Method

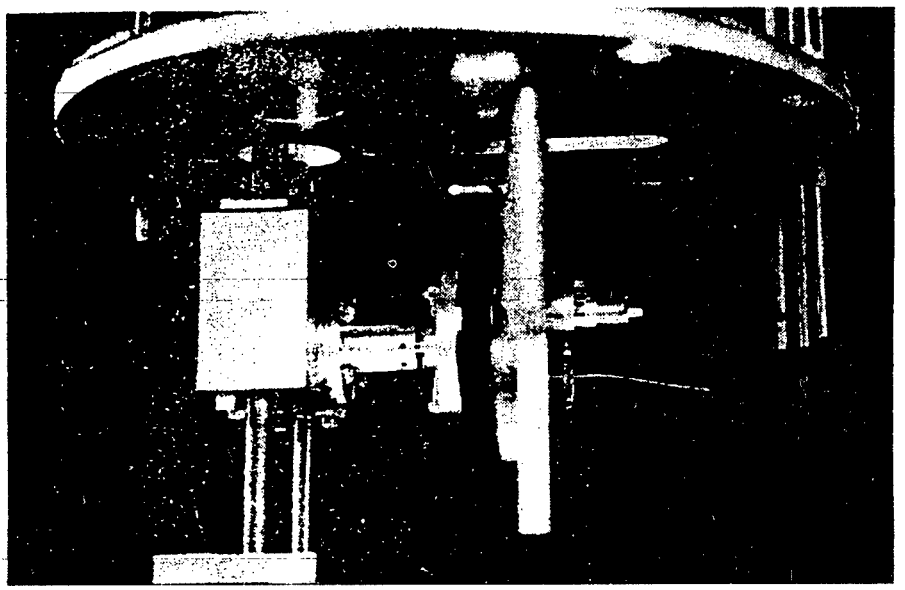

Figure 19. Head of the Micro Heat Flush Device

To produce the local heating, an Argon laser was used as it was assumed to have a high absorption efficiency for the niobium film.

Figure 19 is a photograph of the unit's head. As the measurement data in Figure 20 demonstrates, it was proved that this micro heat flush method is capable of shifting the trapped flux for removal.

To apply this method in an actual device, it is necessary to select a wavelength and a power level that will not affect the characteristics of the device, and also to increase the area of the section to be heated in order to raise efficiency. Further, this method is also effective for removing the flux trapped in the superconductor's magnetic shield. The group was able to establish the basic technology for an ultralow-temperature environment.

Although there are still some problems to be solved, such as improving the pickup coil to upgrade the positioning resolution, it is significant that we could measure

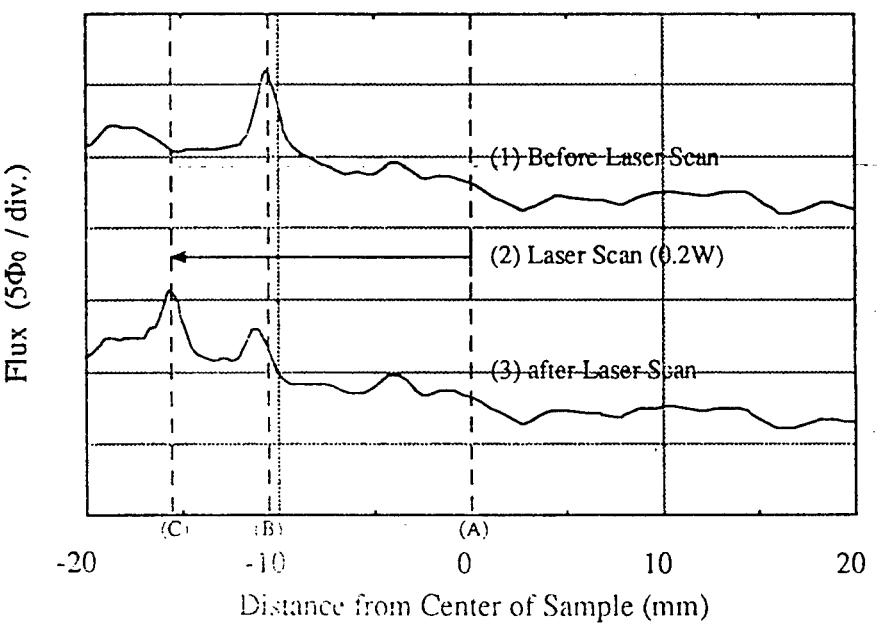

Figure 20. Shift of the Flux by the Micro Heat Flush Method

directly the trapped flux distribution in a superconductive film and were able to remove the flux for the first time in the world.

Further, it is necessary to have an ultraclean room and an ultrahigh vacuum to obtain a clean superconductive film where no flux will be trapped. Therefore, the group studied the characteristics of a vacuum unit based on the cryopump, and produced a vacuum 10 times greater than previous vacuums.

(5) Prospects for the Future

Studies carried out under the auspices of the project have resulted in 34 patent applications in Japan, 14 patent applications overseas, 5 books, 47 theses, and 94 verbal announcements (including some to be forthcoming at the end of June). These are listed in the following article.

Some specific results include a uniform magnetic field generator that is being marketed by Tokin Company, Ltd., but most of the results lie in the area of fundamental research, and they need to be studied further before reaching the development level. Some topics that are approaching the application study level are scheduled to be handed over to a new technology project for further development. To be specific, a high-technology consortium composed mainly of Hitachi affiliates to study QFP devices, and another headed by Japan Vacuum Technology Company, Ltd. to study ultralow magnetic field generation technology are under discussion.

Furthermore, some items that need further fundamental study are scheduled to be handed over to the Goto Special Study Laboratory that was set up in FY 1991 at the Rikken Institute, and to other fundamental research divisions.

We would expect each of the following research areas to offer interesting fundamental research themes:

(i) Thermal limit of QFP, its quantum physical limits, experimental clarification of physical limitations such as flux invasion length in London. In particular, it is necessary to confirm a relationship between speed and the limit of power consumption, and challenging the limits of device downsizing.

(ii) Theoretical study of the QFP device using high-temperature superconductive materials.

(iii) Clarification of the information theory based on the noncalorific energy calculation theory.

(iv) Study of the computer architecture for Peter-FLOPS (floating-point computation at 1 quadrillion times per second).

(v) Study of the flux trapping mechanism.

Meanwhile, the following items are interesting for application research. Of course, further studies will be required to promote the study tasks described in this project to the level of practical development.

(i) Large-scale and high-integration technology for QFP.

(ii) QFP-application circuit design technology.

(iii) Packaging technology such as ultrahigh-speed clock signal distribution technology, focusing on high-speed and high-density circuits.

(iv) QFP/semiconductor mixing technology.

(v) Application of the cyclic pipeline architecture to silicon LSI high-speed operation technology using a new circuit.

(vi) High-performance helium liquification technology.

(vii) Upgrading technologies for removing trapped flux.

In conclusion, we offer our sincere thanks to the New Technology Project Foundation, who helped to establish and to promote this Quantum Flux Information Project, as well as to those who cooperated fully in offering researchers and research sites to promote the project studies during the project period. We extend particular thanks to Hitachi, Ltd., Mitsui Shipbuilding Company, Ltd., Mitsui Shipbuilding System Laboratory, Japan Vacuum Technology Company, Ltd., Alpack Cryo Company, Ltd., and Seiko Electronic Engineering Company, Ltd.

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86-301944	12/18/86	Flux measurement unit	E. Goto Y. Harada	88-153484
87-5486	01/13/87	Fluid vacuum unit	E. Goto	88-173865
87-11085	01/20/87	Superconductive switching circuit	V. Harada	88-179622
87-24356	02/04/87	Superconductive circuit	Y. Harada	88-193612
87-53416	03/09/87	Excitation method for QFP circuit	Y. Harada	88-219220
87-190900	07/30/87	Signal detection method for QFP	Y. Harada	89-35285
87-204781	08/18/87	Fluid compressor unit	J. Yuyama E. Goto	89-53078
87-226202	09/09/87	Superconductive circuit	E. Goto Y. Harada	89-68142
87-258606	10/14/87	Superconductive inductor	Y. Harada E. Goto	89-100980
87-295780	12/24/87	Superconductive A/D converter	Y. Harada	89-137727
88-103449	04/26/88	Superconductive magnetic shield container and method	J. Yuyama E. Goto	89-274498
89-65182	03/17/89	Flux distribution measurement unit	J. Yuyama H. Minami	90-243982
89-65183	03/17/89	Signal transmission method and device	E. Goto Y. Harada	90-244908
89-97763	04/18/89	Logic circuit	Y. Harada	90-276310
89-169110	06/30/89	Uniform magnetic field generator	E. Goto M. Hosoya	91-34501
89-196115	07/28/89	Superconductive threshold logic circuit	Y. Harada	91-60219
89-239219	09/14/89	Flux detection unit	E. Goto Y. Harada	91-102276
89-253091	09/28/89	Ultrahigh vacuum unit	Y. Yuyama M. Kasuya	
89-254205	09/29/89	Highly sensitive fluxmeter	E. Goto H. Nakane	91-115874
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90-170787	06/28/90	Refrigerator	E. Goto Q. Geng J. Yuyama	
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(Domestic Applications) (Continued)

Application number	Application date	Invention name	Name of inventor	Disclosure number
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90-251493	09/20/90	Threshold logic circuit	Y. Harada	
90-251494	09/20/90	Static magnetic field measurement unit	J. Yuyama E. Goto H. Minami Q. Geng K. Chihara	
90-253674	09/21/90	Threshold logic circuit network and learning method	Y. Harada	
91-31075	02/26/91	Threshold logic circuit with reverse dissipation learning function	Y. Harada	
91-49333	03/14/91	Superconductive toggle flip-flop circuit and counter circuit	Y. Harada W. Hioe	
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Pending		High-speed computation of basic function	E. Goto W. F. Wong	

(Overseas Applications)

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USA	146.160	01/20/88	Superconductive circuit	Y. Harada	4.902.908
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USA	274.493	11/22/88	Superconductive A/D converter	Y. Harada	4.956.642
USA	494.987	03/16/90	Flux distribution measurement unit	J. Yuyama F. Naruse H. Minami E. Goto	Patent granted
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USA			Refrigerator	E. Goto Q. Geng J. Yuyama	
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3. Research Report Papers

(1) Fundamental Property Group

Operation Principle of Quantum Flux Parametron (QFP)

Physics of QFP Operation (W. Hioe and E. Goto)

QFP as a Flux Transfer Device (Y. Harada, W. Hioe and E. Goto)

Demonstration of QFP Operation (N. Shimizu, Y. Harada, N. Miyamoto, M. Hosoya and E. Goto)

Logic Circuits

Highly Functional Logic Circuits and Logic Design (W. Hioe, M. Hosoya, E. Goto, R. Suda and N. Miyamoto)

High-Speed Operation of QFP Circuits

Very-High-Frequency Operation of the QFP (J. Casas, R. Kamikawai and E. Goto)

Stability and Microwave Time Domain Testing of the QFP (J. Casas, R. Kamikawai and E. Goto)

Three-Dimensional Packaging of QFP Circuits

Three-Dimensional Packaging Scheme and Its Realization (M. Hosoya, R. Kamikawai, Y. Wada, W. Hioe, E. Goto and T. Tajima)

Analog-to-Digital Converter Circuits

Basic Characteristics of QFP Analog-to-Digital Circuit (N. Shimizu, Y. Harada, N. Miyamoto and E. Goto)

A Quantum Flux Parametron-Based Analog-to-Digital Converter (Y. Harada and J. B. Green)

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Must Information Be Negative Entropy? (N. Yoshida, E. Goto, K. F. Loe and W. Hioe)

(2) Computer Architecture Group

Cyclic Pipeline Architecture (CPC)

Multiple Instruction Streams in a Highly Pipelined Processor (M. Sato, S. Ichikawa and E. Goto)

Evaluation of the Continuation Bit in the Cyclic Pipeline Computer (P. Spee, W. F. Wong, M. Sato and E. Goto)

Effects of Multiple Instruction Stream Execution on Cache Performance (P. Spee, W. F. Wong and E. Goto)

Concurrent Models for the Cyclic Pipeline Computer (P. Spee and E. Goto)

FLATS2

Evaluation of FLATS2 Instruction Set Architecture (S. Ichikawa and E. Goto)

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Perspective for High-Speed Computer

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(3) Magnetic Shielding Group

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Detection and Removal of Flux Quanta Trapped in Superconductor Films

Detecting Flux Quanta Trapped in Superconducting Films by Scanning a SQUID Pick-up Coil (H. Minami, Q. Geng, K. Chihara, J. Yuyama and E. Goto)

Sweeping of Trapped Flux in Superconductors Using Laser Beam Scanning (Q. Geng, H. Minami, K. Chihara, J. Yuyama and E. Goto)

Technique for Measuring Absolute Intensity of Weak Magnetic Fields by a SQUID Pick-up Coil System (Q. Geng, H. Minami, K. Chihara, J. Yuyama and E. Goto)

Magnetic Field Distribution Arising From a Trapped Fluxon (Q. Geng, K. Chihara and E. Goto)

4. Abstracts

Physics of QFP Operation

Willy Hioe and Eiichi Goto

The Quantum Flux Parametron (QFP) is a Josephson device which works on the parametron principle. It operates by holding a single flux quantum in a superconducting loop and transferring signals by flux. Its main characteristics can be understood by analyzing the quasi-static states from its Hamiltonian. Under suitable loading conditions, it has a bistable potential when active, with minima having opposite polarity. It has the high speed of Josephson devices and switching rates in excess of 100 GHz may be expected with low T_c devices. Moreover, because it works only in the superconducting domain, it has a much lower power dissipation than voltage transfer Josephson devices, which allows denser packaging, a property important for high-speed computers.

The QFP operates close to the physical limits determined by thermal hopping and macroscopic quantum tunneling (MQT). The barrier between its potential minima is typically less than 100 kT, where k is Boltzmann's constant and T is absolute temperature. For reliable computer operation at 10 GHz clocking, spontaneous transitions due to thermal hopping and MQT must be less than one in 10^{26} switching operations.

Theoretical analyses on static potentials based on classical diffusion theory provide relationships linking thermal hopping rate to various device parameters such as the device energy, load, activation level, input or reaction, junction capacitance and damping level. Since the potential is not static but varies dynamically with an activation clock, Monte Carlo simulations have been conducted to verify error probability due to thermal fluctuations. A fairly good match was found between the exponential order of the static and dynamic results. However, an analytical treatment of the dynamic stability will still be desirable.

The MQT rate was estimated from theoretical results on static potentials obtained by physicists. Assuming a cubic potential, a closed-form solution can be found which takes into account the effect of damping. The MQT rate for a 10 GHz-level device is much lower than the thermal hopping rate at liquid He temperature. However, if switching speed is increased without increasing energy level, the MQT rate rises rapidly while thermal hopping rate remains roughly at the same exponential level.

The feasibility of operating QFP's at liquid nitrogen temperature is also discussed.

QFP as a Flux Transfer Device

Y. Harada, W. Hioe, and E. Goto

The switching device (flux quantum device), which is a signal carrier of quantized flux in a superconductive state, is described. This paper defines the generalized flux, which is a fundamental concept of the flux quantum device, and, using this concept, the operation of rf-SQUID, which is the fundamental circuit, is described. Further, using them, four quantum fluxes (Quantron, QFP and others) already explained in addition to Fluxon and Thoriton devices are introduced.

Through these descriptions, the quantum flux device characteristics—(1) high gain capability, (2) high-speed performance, (3) low power consumption and problematics, (4) weak load capability, and (5) weak external interface due to low signal power—are discussed.

Further, by picking up QFP, the parametron principle characterizing its operation and the circuit structure realizing its principle were clarified, and examples of QFP studies, frequency divided circuit, and analog-digital converter are introduced.

Demonstration of QFP Operation

N. Shimizu, Y. Harada, N. Miyamoto, M. Hosoya, and E. Goto

This paper presents a recent study of a method for measuring the QFP's fundamental operation, and the application of this method to evaluate the fundamental logic circuit characteristics of the QFP.

The evaluation method for the fundamental digital characteristics detects the QFP output signal using a dc-SQUID. The QFP output current is converted to voltage lineally with the dc-SQUID. Through this method, the relationship between the QFP, the input signal current, the excitation current, and others in the low-frequency domain has been clarified. Further, the basic characteristics of the logic circuit, such as the majority circuit and others, also were confirmed.

These results demonstrate that QFP operations agree well with simulations based on theory.

Further, a new flush-type A/D converter consisting of the QFP and an rf-SQUID was proposed, and its A/D operation characteristics in the low frequency domain have been confirmed. This is a four-bit circuit using the QFP as a comparator. Simulations show that operations at an input bandwidth of 20 GHz can be expected, and confirm the possibility of using the QFP as an ultrahigh-frequency device.

Highly Functional Logic Circuits and Logic Design

Willy Hioe, Mutsumi Hosoya, Eiichi Goto, R. Suda, and N. Miyamoto

The Quantum Flux Parametron is evaluated with respect to logic design. The central component of a computer at

the device level is the family of logic gates that enables one to form all logic functions. Several evaluation criteria are common to all logic gates. To evaluate how fast is a logic circuit built with the gates one considers switching speed, fan-in and fan-out. The functionality, or the complexity of logic that is performed by a single gate, may also be included. To evaluate how complex is the circuit that can be integrated in a single chip one considers size, margin and power dissipation.

An important issue for the QFP is the reduction of gain due to fabrication variations. Low gain affects fan-out as well as the length of lines connecting gates and gate-to-gate interaction. Theoretical and experimental results are given for the booster, an auxiliary circuit that improves gain.

QFP logic families intensively studied so far include the wired-majority gate and the D-Gate. Interaction between active gates and input margin are serious problems for the former. To alleviate these problems the D-Gate was proposed. Implementing the D-Gate required two innovations: a puller to enable the QFP outputs to activate another QFP and an I/O-type QFP which incorporates an I/O transformer into the QFP and simplifies the D-Gate design. Simulations have shown the scheme to be feasible and reduction of interaction and margin problems to be good. However, test chips fabricated so far have not been as successful. Although the basic operating principle was confirmed, design of transformers with good coupling factors remains a problem.

Finally, logic design which exploits the high functionality of the D-Gate and the self-latching property of QFP's is discussed. The D-Gate can form many useful logic functions with a single gate, especially the majority and parity functions needed by full adders. Examples are given for a multiplexer, a shifter, an 8-bit fixed-point adder and a priority encoder. QFP gates are suitable for pipelined logic designs since no penalty is paid for extra latches. They have the potential for very high throughput. However, there are two disadvantages. Since only one gate can be inserted between latches, the propagation delay between gates greatly reduces throughput and clock speed. The contribution of line inductance to load strongly limits line lengths.

Very-High-Frequency Operation of the QFP

Juan Casas, Ryotaro Kamikawai, and Eiichi Goto

QFP shift registers employing four-phase clocking are designed. In order to generate subharmonics of a given clock frequency, one to four single-bit shift registers are cascaded in a closed loop configuration. The clock is obtained by shortening the end of the microstrip clock lines, and is applied as a standing wave. Using this scheme it is observed that for some frequencies, the crosstalk between the output and clock signals is dramatically reduced. The clock current amplitude margin is deduced from the maximum operating frequency of some of the devices; it is at least 17 percent at operating frequencies beyond 5 GHz. The 1-bit device is observed to operate from dc up to 16.2 GHz and the 4-bit shift register structure functions at frequencies over 5 GHz.

Stability and Microwave Time Domain Testing of the QFP

Juan Casas, Ryotaro Kamikawai, and Eiichi Goto

Until recently most of the high frequency measurements related to the QFP have been done in the frequency domain. In this work it is shown that it is possible to sample in time domain the output waveform of a QFP circuit. Crosstalk with the clock frequency and wideband white noise are the main problems to solve. Crosstalk is reduced by using an active cancellation technique. Against white noise a low noise amplifier and an averaging oscilloscope are used. Time domain measurements are done for a single-bit and a 12-bit shift registers working at 5 GHz and 2.4 GHz respectively. The 12-bit device is the largest ever reported device using the QFP (48 QFPs) and it employs an inductive tree for clock power distribution. The 12-bit shift register is also used for demonstrating that 10^{15} error free operations per QFP are possible.

Three-Dimensional Packaging Scheme and Its Realization

M. Hosoya, R. Kamikawai, Y. Wada, W. Hioe, E. Goto, and T. Tajima

This paper describes the three-dimensional packaging of QFP circuits as a method to create the high-performance, high-density packaging that is essential for upgrading circuits. With the QFP, there is an advantage in that it is possible to transmit signals through a magnet junction without direct contact. Therefore, simply by laminating several QFP circuit chips it is possible to effect transformer signal transmission. This function suggests that it is possible to achieve low power consumption and three-dimensional, high-density packaging.

In order to demonstrate these possibilities, we have test-manufactured a fundamental model by laminating two QFP circuit chips to confirm the signal transmission. With this fundamental model, the QFP input/output signals and excitation fluxes were exchanged via transformers located on the surface of each chip. The QFP input/out transformers were designed to suppress transmission signal loss and to remove the effect of external flux.

To assemble and position the two chips accurately, a new three-dimensional package assembly unit was designed and manufactured. By using such techniques as the precision vertical shifting mechanism and concurrent two-point-on-the-chips observation mechanism, a highly accurate positioning unit with a combined accuracy of 3 μm was realized.

We test-manufactured a fundamental model to mount one device chip on the wired chip for evaluation, and, with this model, we confirmed that the input/output and

excitation flux are transmitted in accordance with the design. By further improving this packaging method, a high-density, three-dimensional QFP circuit would be possible.

Basic Characteristics of QFP Analog-to-Digital Circuit

N. Shimizu, Y. Harada, N. Miyamoto, and E. Goto

This paper proposes a new flush-type A/D converter circuit that combines QFP and rf-SQUID.

In the fundamental circuit, the QFP is connected as a negative load inductance of the rf-SQUID, thereby converting the input analog signal to a cyclic digital signal with 1 flux quantum as the cycle. The QFP amplifies the excitation signal by adding, and, at the same time, works as a comparator for the cyclic digital signal. This circuit is expected to have a high-speed operation at 20 GHz in accordance with a simulation.

We have confirmed experimentally the basic operation at 100 kHz by test-manufacturing a four-bit A/D converter having four of the above fundamental circuit using the Nb/Pb process.

A Quantum Flux Parametron-Based Analog-to-Digital Converter

Y. Harada and J. B. Green

This paper reports the experimental results of a high-speed A/D converter using QFP. The A/D converter comprises a comparison circuit consisting of an rf-SQUID and a QFP. Simulations have indicated that this converter should operate faster than any existing device, including a semiconductor device and dc-SQUID-type superconductive device. To confirm this high-speed performance, we have manufactured and evaluated an integrated circuit through the NbN/lead alloy Josephson process with a minimum size of 5 μm and a superconductive current density of 100 A/cm^2. Our evaluation confirmed that the analog signal can be converted to a digital signal up to a frequency of 18.2 GHz. Further, it has been confirmed using the sampling method that a signal with an input bandwidth of 5.4 GHz can be converted. These results demonstrate that this A/D converter has a high-speed capability.

Process Issues of QFP

N. Miyamoto and H. Nakane

The Quantum Flux Parametron (QFP) is a superconductive device using the quantum flux as a logic unit. Therefore, to ensure proper circuit operation, it is necessary to satisfy the requirement that the product of the critical current of the Josephson junction and the inductance value of the superconductive loop be constant. This is necessary to preserve the quantum flux. Thus, it is necessary as a process to control accurately the pattern size and critical current density of the Josephson junction. This paper outlines a QFP manufacturing process, and, at the same time, reports the results of a discussion of the causes of the dissipation of critical current in a Josephson junction.

The QFP manufacturing process involves forming the superconductive wiring (four-layer niobium and lead alloy) with the sputter sedimentation method, and a process for forming the silicon oxide interlayer insulation layer by the vacuum deposition method.

The total number of masks is 14, and the minimum fabrication size is 5 μm, including the superconductive wiring and the Josephson junction. The Josephson junction is formed as a tunnel insulation layer of the niobium oxide layer grown between the second and third superconductive wirings by the plasma oxidation method. To ensure the consistent formations of junctions, sputter cleaning using argon gas was employed in forming the niobium oxide layer together with a low-temperature lift-off process.

Dispersion of the Josephson junction's critical current in the chip can be held to the less than +/- 10 percent required by the device design specifications. However, there is a large dispersion of the critical current value among lots, and the main causes of this dispersion were studied. Four possible causes were identified: (1) dispersion of the Josephson junction's area, (2) natural oxidized film thickness on the niobium, (3) grown niobium oxide film thickness, and (4) the adherence of foreign matter. These were studied experimentally.

As a result of the study, it was assumed that the main cause of the dispersion of the Josephson junction's critical current between lots is the generation and adhesion of foreign matter during plasma discharging, and not the dispersion of pattern sizes or insulation film thickness.

Inductance Calculation System for Superconducting Circuits

M. Hosoya, E. Goto, N. Shimizu, N. Miyamoto, and Y. Harada

This paper describes an inductance calculation method for complicated three-dimensional superconducting circuits. This method approximates a superconductor with several small parallelopiped rectangulars. When the center of each adjoining small rectangular is connected with a branch, a current circuit network is formed by these branches. To designate the individual current distribution of this current circuit network, N-piece cyclic current Ii ($1 <= i <= N$) is selected. Here, Ii is obtained by solving a linear equation system which meets the condition that "at the center of each cyclic current the magnetic field satisfies the London Equation." The inductance is calculated from the sum of the magnetic energy generated among the N-piece cyclic current and the kinetic energy of superconducting electrons. Further, extrapolation is used to save the calculation resource and to improve the resulting accuracy.

Based on this method, an analysis/design system for the superconducting inductor was created by adding preprocessing for shape designation and postprocessing for output. Using this system, we calculated the combined characteristics of the dc superconducting quantum interference device (dc-SQUID) for the logic signal detection. It was confirmed that the calculated value agrees well with the measured value. In the past, inductance by a superconducting inductor with a complicated shape could be obtained only by experimentation, but now it easily can be calculated.

Scaling and Physical Limitations of Quantum Flux Parametron (QFP)

Y. Wada, M. Hosoya, R. Kamikawai, W. Hioe, and E. Goto

The Quantum Flux Parametron (QFP) uses the flux trapped in a superconducting loop as the logic unit. Therefore, ultrahigh-speed operations and ultralow power consumption can be expected. This paper discusses the proportionate scaling and physical limitations, as well as manufacturing bottlenecks for a future QFP supercomputer integrating 10^7 gates on a 1-cm^2 chip.

The proportionate scaling-down rule is applied so that the product of the Josephson junction's critical current and the negative load's inductance equals one-eighth of the quantum flux. By studying the three-dimensional and two-dimensional scaling with a constant thickness, we learned that the switching speed for both becomes 1/k (k: constant of the proportionate scaling).

For the QFP, which is different from an ordinary silicon semiconductor or a voltage-logic-type Josephson device, the power consumption does not serve as a scaling limit, and the device can be downsized to the minimum 0.04 μm. However, it is necessary to evaluate accurately the downsizing limit due to the London equation's invasion length, thermal noise, quantum effect, etc. Further, it is technically possible to control the dispersion of pattern sizes and the Josephson junction's tunnel oxide film thickness adequately, and these factors will not hamper downsizing of the device in the future.

When the above results are combined, it becomes clear that there is no physical problem in manufacturing a QFP supercomputer with a minimum fabrication size of 0.35 μm capable of operating at more than 100 GHz at 4K by integrating 10^7 gates on a chip of 1 cm^2 using the current niobium material. Further, it is possible to operate a supercomputer of the same size at 77K using a high-temperature superconductor when a proper device constant is selected.

Signal Interconnection in Highly Integrated QFP Chips

R. Suda, R. Kamikawai, W. Hioe, M. Hosoya, and E. Goto

One of the biggest problems in designing VLSI is the wiring between the logic devices. As the QFP uses flux as the signal, its wiring is quite different from those of conventional devices. This paper evaluates analytically the limitations and possibilities of signal wiring in large-scale QFP circuits.

There are two main issues related to wiring between QFPs:

(1) Because the QFP is driven by a clock, the length of the wiring directly affects the clock rate. In particular, as the QFP clock is much faster than the clocks of other devices, the wiring length must be minimized.

(2) As the QFP uses a quantum flux as its signal, the wiring inductance is significantly limited. To obtain a proper inductance, the QFP wiring often must be wide, thus requiring wider wiring area than other devices.

For the second of these two issues, it is known that there is a theoretical upper limit for the wiring length. In a typical case, where the wiring length is l, the gate interval is D, P = l/D, and P the mean square of p for all wirings, the limitation comes in the form of $P \leqq C$. Here, C is a function of the output inductance and the wiring inductance for each length, and it becomes a constant when the process is determined. In the present process, C is approximately 25.

If the wiring poses a problem, then it is acceptable to create a wiring circuit that would allow a high inductance. Although some such circuits have been proposed, they suffer from a shortcoming in that all of them are adversely affected by external noise. Further, when they are applied in practice, the limit imposed by the clock rate makes it impossible for the wiring to be long.

Rather than devising a special wiring circuit, a design methodology that makes it possible to determine a range that will satisfy each of the two limits would be a step in the direction of a practical solution.

Against this background, this paper proposes two methods for solving the problem of wiring limitations. These methods are based on the fact that the QFP is not affected in its throughput by the number of logic stages, because of its latch logic. In the first method a buffer is inserted into devices that require long wiring. By inserting the right number of buffers, it is possible to reduce both the wiring length and its mean square as needed. That is, it has been proven that it is possible to realize any logic design with the QFP by inserting buffers properly. In the second method, the bits are divided into several blocks for custom designing of each block. This method requires new designs for each process condition, but has an advantage in that the wiring capability can be used to the utmost. The third method is a design with systemic arrays. By repeating cells with simple functions, it becomes possible to achieve a high throughput circuit by shortening the wirings. Analyses of this configuration have shown that the wiring limitation can be overcome without fail if the number of gates included in the cell is

less than 10. Under these conditions, all of the main configuration devices of a computer—such as the arithmetic function, encoder, decoder, PLA, and memory—can be realized. However, control circuits may not be suitable for the systemic array as they are generally too complicated. In this case, it may be necessary to use buffers.

Studies on an architecture and memory that take wiring limitations into account will be essential for the upcoming tasks. Further, it also will be necessary to study how wiring limitations can be reduced by three-dimensional packaging.

Highly Sensitive Magnetometer

Juan Casas and Eiichi Goto

This paper presents a magnetic flux sensing device that is made by using two dc Squids. The dc Squids are of similar characteristics, magnetically coupled by a common coil and are tuned into the voltage state by a single dc current source. As the dc Squids are magnetically coupled, the magnetic flux noise generated by one of the dc Squids is sensed by the other one and vice versa. Then by making a differential measurement across both dc Squids, the magnetic flux noise detected by the dc Squids can be added either constructively or destructively. This means that magnetic flux noise cancellation is possible as it is demonstrated experimentally. The double dc Squid configuration can also be used in the add flux noise mode, in which case there is no loss of performance when comparing with what is possible to obtain with a single dc Squid. Another non-negligible advantage of the two dc Squids configuration is that the output impedance is twice as large as that of the dc Squid with Josephson junctions of same critical current and shunting resistance. Then in the former configuration the matching to room temperature electronics is simplified.

Must Information Be Negative Entropy?

N. Yoshida, E. Goto, K. F. Loe, and W. Hioe

Using a Josephson computation device, we studied the fundamental issue of the physical limitations imposed by heating during computation. We concluded that it is possible to compute approximately without calorific energy when the QFP is used.

Brillouin's negative entropy hypothesis, "information is negative entropy," and, further, the hypothesis of Keyes, Landauer, and Bennett that the "disappearance of one bit of information causes a loss of calorific energy equal to $\varepsilon = kT \ln 2$" can be rebutted by the following physics discussion using the Josephson computation device as its proof. First, although it is generally held that the Josephson computation device keeps information unvariable even though temperature is lowered intentionally, the third law of thermodynamics says that entropy approaches zero as temperature nears absolute zero. Second, although the calorific value ε has to be calculated accurately as a generated value separate from the heat (entropy) shifting, it has been confirmed with the QFP that it is possible to have calorific energy in a thermodynamic static process which is the limit of the computation rate zero by evaluating such a genuine calorific energy with a simulated computation, even if information is lost.

Based on these studies, we have concluded that information is not negative entropy, and that there is no universal relationship between the disappearance of information and calorific energy.

Multiple Instruction Streams in a Highly Pipelined Processor

M. Sato, S. Ichikawa, and E. Goto

The cyclic pipeline method avoids deterioration of performance due to dependency on instructions in each instruction stream by sharing a highly pipelined processor in time division with multiple instruction streams to improve throughput.

This paper defines a cyclic pipeline computer model and compares it to conventional single instruction stream computers with similar pipelines.

With the cyclic pipeline system, overhead due to parallel execution causes performance to deteriorate. Simulations have indicated that it is possible to raise the efficiency of the entire processor not only by increasing the number of instruction streams but also by carefully executing instructions in the instruction streams in parallel when the parallels are not numerous enough. The FLATS2 is a cyclic pipeline computer with two instruction streams. The FLATS2 is designed to have a better micro architecture, such as BL addressing, for speeding each instruction stream, and the results of an evaluation are given. With the present silicon device, the number of pipelines is limited, but the cyclic pipeline system suggests that a highly pipelined system is appropriate for new devices such as the desirable Josephson logic device.

Evaluation of the Continuation Bit in the Cyclic Pipeline Computer

Paul Spee, Wong Weng Fai, Mitsuhisa Sato, and Eiichi Goto

The Cyclic Pipeline Computer (CPC) is a shared resource computer which shares its pipeline among multiple instruction streams to create distinct virtual processors. This effectively removes data dependencies which reduce the performance of highly pipelined computers.

If a parallelized program is well balanced, that is, the execution times of the instruction streams between synchronization points are nearly equivalent, the CPC obtains a good performance. However, if instruction streams are required to wait at synchronization points, performance may decrease. To improve the performance of ill-balanced parallel programs, we introduce a *continuation bit* as part of the instruction to specify whether

data dependencies between the current and next instruction within an instruction stream exist. If no dependencies exist, instead of issuing an instruction from another instruction stream, the next instruction from the same instruction stream is issued.

The value of the continuation bit is determined at compile time. Based on the operation latency and the number of instruction streams (m), the compiler can determine whether it is safe to set the continuation bit. If the continuation bit is set, the time until the issue of the next instruction is one cycle. If the continuation bit is not set, the time until the issue of the next instruction is at least m cycles. The continuation bit exposes the full pipeline depth to the instruction stream.

Synchronization code does not have the continuation bit set; it passes control to the next instruction stream. As a result, it allows the instruction streams which did not yet reach the synchronization point to execute faster at the cost of the synchronizing instruction streams. Although each stream on the CPC executes one cycle per *turn*, each stream on the CPC with continuation bit will execute on average more than one cycle per turn. Upon reaching the synchronization code, the first instruction stream to reach the synchronization code will execute that code at the rate of one cycle per turn. If the other stream is executing more than one cycle per turn, that stream will reach the synchronization point faster than when it would execute only one cycle per turn. The continuation bit is better able to exploit the available instruction level parallelism. If the CPC is superpipelined, very little instruction level parallelism remains to be exploited by the continuation bit.

Effects of Multiple Instruction Stream Execution on Cache Performance

Paul Spee, Wong Weng Fai, and Eiichi Goto

In recent years, there has been a trend toward multiple instruction stream computer architectures. The Cyclic Pipeline Computer (CPC) is an early example of a statically scheduled multiple instruction stream computer. It shares its pipeline among multiple instruction streams in a time-share manner. The advantages of such machines are that they are capable of hiding latencies, in particular memory access latencies. However, if these instruction streams share a common cache, the cache behavior is adversely affected because the memory access pattern is not characterized by one working set, but by a combination of working sets.

Simulations indicate that when the number of instruction streams sharing a single cache increases, the cache miss ratio sharply increases. The commonly used *bit extraction* set mapping function does not distribute the addresses over the sets very well. Using a modification of the folding method, the addresses were much better distributed over the sets. Associativity is more important as a means of improving performance in multiple instruction stream execution than in conventional single stream execution where a direct mapped cache often suffices.

As technology improves, making it possible to design deeper pipelines, inescapable limitations, in particular instruction level parallelism, will make fine grain, multiple instruction stream execution attractive. The cache, being a proven cost-effective means of overcoming the memory bandwidth limitation, will also play an important role in such architectures. Our studies, by revealing the interactions between the two, will be useful in the future design of fast, deeply pipelined, multiple instruction stream computers.

Concurrent Models for the Cyclic Pipeline Computer

Paul Spee and Eiichi Goto

This paper presents two concurrent programming models for the Cyclic Pipeline Computer. The Cyclic Pipeline Computer implements a tightly coupled MIMD computer by time sharing the processor and the main memory among multiple instruction streams. The *Control Flow Dependency Model* supports concurrency by having multiple jobs with the execution of each job being controlled by the completion of other jobs. The Control Flow Dependencies Model, based on Dongarra's SCHEDULE, allows easy parallelization of non-scientific applications. The basic unit of execution is a job. The request to schedule a job represents the execution of a subroutine call (it does not return a value), except for the fact that the request returns directly, while the job may be scheduled later. The request also includes the arguments with which the subroutine is called. Control flow dependencies may be optionally specified for each job to represent the order of execution. A job is executable if all control flow dependencies for that job have been resolved; in such a case, the job is placed in a queue for executable jobs. The dependencies are called control flow dependencies because they specify the order of execution.

The *Shared Variable Model* is a synchronization model which provides both fine grain synchronization, communication, and scheduling. By associating a full/empty status with a variable which is shared by multiple processes, communication and synchronization are integrated. By adding this model to a language and having the compiler generate and optimize the synchronization, synchronization overhead is minimized. The low synchronization overhead of a Cyclic Pipeline Computer allows efficient implementation of fine-grain synchronization.

Evaluation of FLATS2 Instruction Set Architecture

S. Ichikawa and E. Goto

The FLATS2 is a cyclic pipeline computer based on silicon technology. This paper describes the instruction

set architecture for FLATS2 and the results of an evaluation. The FLATS2 processes extensive array computation applications efficiently by sharing the addressing mode, and features a range inspection (BL addressing mode) and multiple operational instruction. In the BL addressing mode, a range inspection of effective addresses is executed for the base/limit address register couple designated by instruction in computing addresses, and conditional branching is executed within one instruction cycle depending on the range instruction result. This mechanism is suitable for many applications, including the optimization of loops. Further, the FLATS2 achieves a high operational performance by adopting a multiple instruction system for executing several arithmetic operations with a single instruction. This paper shows the application policy of this system together with the results of a performance evaluation based on representative benchmark testing.

Overview of FLATS2 Software System

N. Fukazawa, M. Sato, and P. Spee

This paper presents an overview of the development of software for a test model of the FLATS2 using the cyclic pipeline system. We designed and created a preliminary kernel for verifying and evaluating operating system hardware, as well as a CPX operating system so that users are able to use its multiprocessor, which is based on the cyclic pipeline system. Further, we manufactured a development tool for many programs to make it possible to develop, execute, and debug FLATS2 programs. Through developing these programs, we were able to evaluate the functions of the FLATS2 and to create an environment in which to use them effectively.

The Design and Implementation of the CPX Kernel

Paul Spee, Mitsuhisa Sato, Norihiro Fukazawa, and Eiichi Goto

The CPX kernel is an operating system kernel for FLATS2, a two instruction stream Cyclic Pipeline Computer (CPC). The kernel separates the unit of execution from the environment, allowing multiple threads of control to execute in a single virtual space. It is based on the object-oriented programming model and its components are defined in terms of objects. Ports are required to implement objects. Therefore, all operations on ports are implemented as virtual instructions. These include the creation and deletion of a port; and the sending and receiving of messages. Messages can be either *typed* messages or *untyped* messages.

The kernel defines the virtual machine (VM). The virtual machine consists of the virtual processor (VP), the virtual space (VS) and the virtual cache (VC). Each is implemented as a kernel object. The kernel defines the *operations* on the kernel-defined objects. The virtual processor is the virtualization of the real processor. The virtual processor will hide details of the hardware implementation. Such details also include the number of physical processors the CPC consists of (FLATS2 implements a two processor MIMD). Low level scheduling is done on a *self-service* basis: each processor will schedule a virtual processor from the pool of virtual processors. The virtual space hides the details of the virtual memory implementation. The FLATS2 has a single virtual space, a fact which is hidden from the user by the virtual space implementation. The virtual space not only provides the address space for the virtual processors, but represents the complete environment in which virtual processors execute. When a virtual processor creates a port, the ownership of the port is assigned to the virtual space in which the virtual processor is executing. Modern computer systems implement cache memories as high speed buffers between the processor and the main memory. The access time to the cache memory is much less than the access time to main memory. The virtual memory of FLATS2 is much larger than the physical memory. The memory manager has therefore to decide which pages of virtual memory to keep in physical memory. Page replacement is based on the Least Recently Used (LRU) algorithm. The virtual cache represents the usage of the physical memory. With each virtual cache, there is an associated memory object. The virtual cache represents the pages in physical memory, which contain data associated with that object. Its function is similar to the function of a real cache.

FLATS2 FORTRAN Compiler

M. Sato and E. Goto

An overview of the FLATS2 FORTRAN compiler and its optimized algorithm are presented here.

The compiler converts the intermediate code into a static single assignment (SSA) for optimization by deleting redundant codes, such as common equations and variables in unvariable loops. The SSA style is an expression style of effective programs in optimizing programs.

The FLATS2 has a complicated instruction set and register set. Each instruction is designed to have high-level functions. This is made possible by optimizing peep holes using the instruction-level DAG.

Further, in assigning registers, a local assignment based on information from an extensive register assignment algorithm makes it possible to select an optimum instruction for referring to variables together with the register assignment. These programs are realized with an algorithm that is independent of the machine and designed for easy transfer.

Loop Optimization With BL Addressing

M. Sato, S. Ichikawa, and E. Goto

This paper describes a code creation technique using BL addressing performed by a compiler. The FLATS2 is provided with an addressing mechanism that combines memory addressing, called BL addressing, and the range

inspection for a high-speed array calculation in arithmetic computations. Using BL addressing makes it possible to remove the overhead of loop through its concurrent access to the array in a specific notch width, and judging the loop end also becomes possible.

To apply BL addressing, it is necessary to have a program conversion to delete the inductive variable for accessing the array element by incrementing the pointer. This conversion sometimes will generate many temporary variables. Therefore, our algorithm is designed to trade off the high speed achieved by the BL addressing against the cost of storing these temporary variables in the memory.

The FLATS2 removes the branching loss that otherwise would accompany the BL addressing thanks to its cyclic pipeline system, and, as a result of the benchmark evaluation, a high speed of 10 to 30 percent can be obtained. Since scientific and technical calculations feature many simple and regular array computations, the BL addressing system offers a significant effect.

Dynamic Range Checking in C for the FLATS2

Paul Spee and Eiichi Goto

Runtime checking in general and runtime array subscript checking in particular is considered to be very costly in terms of execution speed. *BL-addressing* allows range checking to be done in parallel with the memory access, thus reducing or removing overhead caused by range checking.

Each word consists of a 32-bit data part and a one-bit address tag. The tag specifies whether the word is to be treated as a 32-bit integer or a 32-bit address. The tag is therefore referred to as the *address tag*. Both memory and the general purpose registers are tagged. If an even and odd numbered general purpose register both contain a valid address, they can be used as a *base* and *limit* register pair. Depending on the memory addressing mode, a general purpose register is either treated as the base or limit register of a BL-register pair, index register or pointer register. For each memory reference a BL-register pair must be specified. The effective address is checked against the base and limit registers. The memory access fails if the base, limit or effective address is not a valid address or if the effective address lies outside the range specified by the base and limit registers. Like capability based systems, only instructions related to address calculation can set the address tag. All other instructions clear the address tag. This protects the user from forming an illegal address. Furthermore, new addresses (and subsequent BL-pairs) can only be derived from existing valid addresses and BL-register pairs.

The current ANSI C definition is insufficient to allow optimizations on arrays such as vectorization and dynamic range checking. To successfully implement dynamic range checking, the declaration of a "pointer to a variable size array" must be explicitly allowed.

In the FLATS2 C compiler, pointers are implemented as addresses. By doing this, the BL-addressing scheme provides a form of dynamic type checking. Arrays are implemented as a BL-register pair. The beginning of the array is specified by the base register, while the end of the array is specified by the limit register. All memory accesses to the array are done using the BL-register pair specifying the array. If the effective address lies outside the array boundaries, a trap occurs.

Using aggressive optimization, most of the overhead associated with BL-register generation can be removed. The execution of benchmarks indicates that including range checking does not increase the execution time. Moreover, using specific features of BL-addressing, loops may be further optimized.

Optimization of Arithmetic Operation by Combined Instruction in FLATS2

S. Kawakami, S. Ichikawa, and E. Goto

The FLATS2 is provided with many special instructions for arithmetic operations to speed up numeric and symbolic computations. With the FLATS2, each instruction has 10-stage pipelines, and, when the DP operation unit is used, two memory accesses (read and write) are allowed for each instruction. Further, the maximum four computing units can be operated in double precision, while eight units can be operated in single precision per instruction, respectively, in parallel. With this capacity, one instruction includes various operations, which makes it possible to package special instructions having high-quality functions. By combining these instructions and the BL addressing, complex number and matrix computations can be executed effectively. To verify the effectiveness of these special instructions, the speed of programs using these special instructions was measured to show the effectiveness of its optimization.

The evaluation was made on a one-dimensional double precision real number inner product, a single precision complex number inner product, a double precision complex number inner product, and complex number FFT computation routines.

With the real number inner product and single precision complex number inner product computation routines, the innermost circle loop consists of one instruction. This is achieved by using the real number inner instruction and the single precision complex number inner product instruction. With the double precision complex number inner product and the complex number FFT computing routines, the innermost circle loop consists of two instructions—the double precision complex number inner product instruction and the FFT instruction. For the single precision, double precision one-dimensional complex number inner product function, and the one-dimensional real number inner product function, the required time for each routine was evaluated about the array element N = 10,000. For the FFT computing subroutine, the number of samples was N = 1,024.

The program used for evaluation was written in FORTRAN for each machine, and optimized with each compiler. The FLATS2 was further optimized by hand coding using a special instruction for arithmetic operations. When a special instruction is used, its effectiveness is remarkable in the complex number inner product computation. As the FLATS2 floating-point arithmetic unit is made for double precision, the number of instructions for double precision and single precision is not very different when codes are created with a compiler. However, as the arithmetic unit can be used effectively depending on the precision of the double number inner product instruction, its effectiveness is notably higher in the single precision.

Even with a relatively complicated operation such as the double number inner product, it is possible to compute at a speed similar to the real number inner product computation. Because the single precision inner product computation can be composed of one instruction, like the real number inner product computation it can make the most of the arithmetic units. The FFT computation has a relatively complicated loop structure, and the ratio of the innermost circle loop is not as high as that of the inner product computation.

However, a significant level of effectiveness is visible among all functions. This is due in part to a tabulation of trigonometric functions.

By combining the above special instructions with BL addressing, the complicated innermost circle loop can be structured with one or two instructions, thereby contributing to high-speed operation.

Fast Hardware-Based Algorithms for Elementary Function Computations

Wong Weng Fei and Eiichi Goto

We propose a set of hardware-based algorithms for the computation of elementary functions which are fast and accurate. The algorithms themselves are derived from well identities. What is new is as follows:

1. Byte multiplication is used. We note that in many instances, it is not necessary to perform full multiplication. In such cases, byte multiplication gives us twice the speed of a full multiplication at a fraction of the cost.

2. Fixed point arithmetic is used. Fixed point arithmetic is significantly faster than floating point one especially if only short precision is required.

3. Parallel operations are performed. Unlike typical software algorithms, microscopic parallelism in algorithms, too expensive to be exposed by software, are harnessed at the expense of adding more hardware.

4. Tables are used to further speed up the convergence of the algorithms.

5. Truncations based on accuracy of the data values are used extensively to reduce, say, the number of Taylor terms required.

6. Partial operations are performed when the full result is not needed.

7. Specialized hardware is employed to fuse together certain operations.

The above are some of the main ideas involved in all our algorithms. However, specific to each algorithm, there are some tricks which can be used to speed up convergence.

Six Basic Benchmark Problems for Number Crunchers

Wong Weng Fai, Eiichi Goto, Yoshio Oyanagi, and Nobuaki Yoshida

The problem of estimating the performance of computers, traditionally known as *benchmarking*, aims to provide a realistic picture of a computer system's performance under normal operations. This is particularly important in the field of supercomputing where the investments in hardware resources are substantial. One of the major uses of supercomputers is in scientific computing which are basically computation intensive, numerical calculations. *Supercomputer* is the name given to the class of pipelined, vector processes which are designed specially with scientific computing in mind. Our proposal calls for maximum freedom for the benchmark programmers within the constraints of the given problem. The programmers are given freedom in selecting the language, programming style, algorithm and optimization necessary to get the best performance for solving the given problem on the given machine. Performance is measured in terms of number of outputs per unit time or time taken to produce a specified unit of output. We propose six basic problems which we think:

1. Reflect the nature of scientific computing in that they are fundamental and frequently used;

2. Reflect the chaining mode of the ALUs which is by far the most important architectural feature of any supercomputer;

3. Reflect the memory accessing capability of the machines.

The six basic problems are: (1) Random Number Generation; (2) Elementary Function Generation; (3) The Fast Fourier Transform; (4) Dense Matrix Computation; (5) Rule-Specified Sparse Matrices; and (6) List-Vector-Specified Sparse Matrices. We believe that the above problems represent a significant cross-section of fundamental scientific computations and that by allowing the programmers to exercise total freedom in coding the programs to solve these problems, we would have a set of benchmark figures that would reflect better the underlying architecture of the given machine. In addition, we propose three additional tests which we call the *modular dip, memory hierarchy and burst mode* tests.

These three tests are meant to highlight subtle hardware characteristics not exposed by the six basic problems.

New Approach for High-Efficiency Pulse-Tube Refrigerator

J. Yuyama, M. Kasuya, M. Nakatsu, Q. Geng, and E. Goto

A highly reliable, ultralow-temperature refrigerator capable of continuous operation for long periods of time is essential to cool a computer that uses superconducting devices such as the QFP.

Therefore, we took note of the pulse-tube refrigerator and studied how to upgrade its performance. The pulse-tube refrigerator does not have any moving parts in its ultralow-temperature section, and this is very advantageous in terms of reliability.

In the past, the cooling mechanism of a pulse-tube refrigerator was believed to be due to a heat exchange between the pulse-tube wall and the interior gas. However, some recent studies have disclosed a work flow flux in addition to the heat flow flux in the pulse tube. If this phenomenon is extrapolated, one reaches the point where there is no heat exchange between the pulse-tube wall and the interior gas, but only the work flow flux is transmitted in the pulse tube. In this case, the gas in the pulse tube is assumed to function as an "extended piston" transmitting the expansion work generated in the ultralow-temperature section to the piston in the room-temperature section. In this way, the work flow flux in the pulse tube is important in developing the mechanism of pulse-tube refrigeration, but it has not been studied sufficiently in the past.

Therefore, we tried to study the relationship between the work flow in the pulse tube and refrigeration capability. To that end, we test-manufactured a new pulse-tube refrigerator with a piston attached to the end of its room-temperature section. With this method, the work flow in the pulse tube could be controlled by the movement of the piston at the end of the room-temperature section, and the volume of work that reached the room-temperature end could be measured as well. Also, when the timing of the piston is varied, the phase difference between the gas displacement and pressure fluctuation in the pulse tube changes. When the piston stroke is varied, the gas displacement volume (flow rate) changes. Further, both can be changed independently. This feature is not available with the basic conventional or orifice-type pulse-tube refrigerator. Although an irreversible process is essential for operating conventional basic or orifice-type pulse-tube refrigerators, the new piston-type pulse-tube refrigerator does not need the irreversible process, which is advantageous for efficiency improvement.

Our experiments with the piston-type pulse-tube refrigerator made it possible to identify the following characteristics:

First, as the workload absorbed at the room-temperature end piston is increased, the attainable temperature is lowered. That is, the absorption of work by the room-temperature end piston contributes to improving the refrigeration capability. In contrast, when the workload is added to the gas by the piston, the attainable temperature rises.

Second, in an operation where the attainable temperature is about 140K, the refrigeration capability in a relatively high temperature range will be higher than the workload absorbed by the piston. This shows that part of the expansion work generated at ultralow temperatures is discharged externally as heat before it reaches the piston at the room-temperature end.

Third, the rate at which the attainable temperature rises in accordance with the decrease in absorption work due to the piston is greater than that of the attainable temperature rise due to the calorific energy added by the heater in the ultralow-temperature section. This indicates that the refrigerator capacity increases when the absorbing workload is raised, while the calorific energy discharged externally decreases. Therefore, an effective way to realize a pulse-tube refrigerator with a large refrigerating capacity is to absorb the expansion work generated in the ultralow-temperature section as work.

Fourth, it is possible to operate the piston at the room-temperature end at a lower frequency than for the orifice-type, and we were able to reach 70K with an operational frequency of 1.3 Hz.

Entropy Production Analysis of Refrigerators

Qiquan Geng, Junpei Yuyama, and Eiichi Goto

This paper examines how the entropy is generated in a refrigeration system and looks at what the parameter dependences of those losses are, why the refrigeration power per unit mass flow rate in a refrigerator is usually small, how to reduce the entropy production in refrigerator and how to increase the refrigeration power per unit mass flow rate. Based on the theoretical analysis, a modified version pulse-tube refrigerator is suggested. Additional ways to improve efficiency of refrigerators are also proposed.

Reduction of Maximum Principal Stress by Multilayering Electrodeposited Bellows

K. Chihara, M. Kasuya, J. Yuyama, and E. Goto

A refrigerator with a fully closed cycle needs a bellows. However, a refrigerator that uses a bellows is handicapped by the fact that its service life is shorter than other refrigerators, since a bellows causes destruction due to metallic fatigue. When the problem of fatigue destruction is solved, it will be possible to produce a highly reliable refrigerator, because it will have a fully closed cycle.

To eliminate destruction due to metallic fatigue, it is necessary to minimize the stress generated in the bellows

as much as possible. For this purpose, we thought that a multilayered bellows with soft and hard laminated materials would be effective in minimizing stress. To verify whether such a bellows would actually reduce stress, we analyzed the stress created in this bellows using the finite element method. At the same time, we analyzed the stress in a single-layered bellows and a multilayered bellows made with a molding method and compared the stresses generated in these bellows.

In order to examine the stress pressure generated in these bellows, or the dependency on their deformations, we analyzed three cases—where only pressure (2.53×10^5 Pa) is exerted on the bellows, where deformation occurs without pressure (expansion of 7.5 percent), and where deformation and pressure are applied concurrently. Further, we analyzed the bellows using as parameters the Young's modulus ratio ($1\text{-}12^5$) of the soft and hard materials used for the electrodeposited layer bellows and their hard layer ratio (0.21-0.71) to examine conditions where the stress generated in the electrodeposited bellows is reduced. With deformation set at 7.5 percent (extension) and pressure at 2.53×10^5 Pa, the effect of stress on the wall thickness of all three bellows was examined. The Young's modulus for the electrodeposited layer bellows was fixed at 10^2, and the hard layer thickness at 200 μm. The stress generated in the multilayered bellows shrank to 16 percent less than that of the single-layered bellows, while the stress in the electrodeposited layer bellows was reduced by 10 percent.

These analyses demonstrated that the stress generated in the electrodeposited layer bellows can be reduced by as much as in the multilayered bellows, and more than is possible in a single-layered bellows.

Fatigue Strength of Electrodeposited Nickel Films

M. Kasuya, K. Chihara, J. Yuyama, and E. Goto

It is essential to have a highly reliable ultralow-temperature refrigerator that is capable of running continuously for long periods of time to cool computers that use superconducting devices like the QFP.

When a bellows is used as the expander in an ultralow-temperature refrigerator, the work flow (usually helium gas) can be completely sealed against foreign matter to improve the reliability of the refrigerator. However, the breakdown of the bellows due to metallic fatigue makes it hard to realize a refrigerator with a long service life.

Therefore, we came up with a system for reducing the stress generated in the bellows wall by forming the bellows through a sequential electrodeposition of two hard and soft metals with a different Young's modulus, and analyzed the effect of stress on this bellows using the finite element method. It is necessary to make the most of these analyses to understand the fatigue strength of electrodeposited nickel films and thereby estimate the service life of a bellows-type expansion unit.

Therefore, we examined the fatigue characteristics of electrodeposited nickel films. Since electrodeposited nickel films are used widely for the components of bellows other than the laminated electrodeposited bellows described above, the testing results of the fatigue strength of these bellows are useful data.

We measured the fatigue strength of electrodeposited nickel films as thin as 2 to 30 μm. To examine the mechanical characteristics of a thin electrodeposited film, it is essential to avoid the effect of an end section, and to apply a uniform stress. When a foil-like sample is used, it is possible that the fatigue strength may appear to lower as cracks are generated from various defects at the end section. Therefore, a thick cylindrical sample from the electrodeposited nickel film was prepared for the fatigue test.

The electrodeposited nickel film sample was made using a sulfamine acid nickel plating solution. Its inner diameter was 8.8 mm, its length was 50 mm, and its thickness was 30 μm.

The thickness dispersion of the samples was evaluated using six samples made in similar conditions. The standard deviation from the average thickness of the samples was 2.0 μm. This indicates that a cross section of the samples (including stress value) can be evaluated within a range of +/- 7 percent.

The evaluation of the fatigue limit (time strength of 10^7 times) was performed using the staircase method as set out in the Japan Machine Society Standard. First, 10 broken-down samples were aligned linearly on the S-N line graph, and a standard deviation of 23.7 MPa was obtained. Based on this value, the step width was set at 20 MPa for the staircase test. From the results of this test, which is 95 percent reliable, we can assume that the interval of fatigue limit stress amplitude is 150.5 +/- 22.3 MPa.

Finally, we examined the relationship between the condition of the sample surface and the fatigue strength. Thanks to an improved method for grinding the surface of the samples, we were able to produce samples with little surface roughness. The average surface roughness before the improvement was 0.49 +/- 0.17 μm, but became 0.20 +/- 0.09 μm after the improvement. When compared on the S-N line graph, there is no significant difference between them in terms of fatigue strength, and it is known that the difference in surface roughness is not the major cause of fatigue strength dispersion.

Detecting Flux Quanta Trapped in Superconducting Films by Scanning With a SQUID Pick-up Coil

H. Minami, Q. Geng, K. Chihara, J. Yuyama, and E. Goto

Many methods have been developed to detect flux quanta trapped in superconducting films. However, these methods can detect only flux quanta trapped in the

electrode section of the Josephson junction, and detection within a microvisible area only was possible.

Therefore, we developed a new method—detecting trapped flux quanta by using the detection coil of a SQUID fluxmeter to scan the surface of superconducting films. With this method, we succeeded in detecting flux quanta trapped in superconducting films.

The fundamental principle is as follows:

The main axis of the detecting coil is vertical to the surface of the superconducting films. Near the superconducting film surface, the external magnetic field runs parallel to the film surface by virtue of the Meissner effect, and does not have a component vertical to the surface.

Meanwhile, in the section where the flux quanta are trapped, the magnetic field has a vertical component near the trapped flux quanta, because the flux is blowing out from the surface. Therefore, when the coil is scanned from a section without a trapped flux toward the trapped flux, the fluxmeter signal changes near the trapped flux, although there is no change in areas where there is no trapped flux. When the coil is placed adjacent to the surface of a superconducting film that is sufficiently large compared to the coil diameter, and when it is scanned toward one of the trapped flux quanta, a signal change equivalent to Φ_0 is observed directly above the flux quanta.

The actual detection of flux quanta is done in liquid helium (4.2K). In an experimental unit that we manufactured, the detection coil and a superconducting sample (Nb film) were placed in helium, and the entire cryostat was housed in a triple-sealed permalloy shield. The detection coil is a magnetometer type with a Ni-Ti wire 80 μm in diameter wound around a 1-mm crystal bobbin. The clearance between the coil and the sample is about 100 μm. The coil is scanned by rotating or moving up and down the sample. Power is supplied by a motor mounted on top of the cryostat.

Further, since nonuniform magnetic fields caused by magnetized experiment instruments and component materials increases the quantity of trapped flux quanta, thereby making it impossible to detect a single flux quantum, nonmagnetic materials such as aluminum alloys are used, especially near the sample.

As described above, this magnetic field measurement system is highly sensitive to trapped flux quanta, but is not sensitive to the external magnetic disturbance. We have verified this phenomenon experimentally. Our magnetic field measurement system has a flux detection sensitivity of $< 0.1\ \Phi_0$ and a positioning resolution of $<<$ 100 μm. Further, the effect of external magnetic disturbance on the detection coil is about 20 percent of the external magnetic field change.

With an experimental unit capable of this level of performance, we measured the magnetic field distribution on the surface of a superconductor. During this experiment, the SQUID fluxmeter observed many peaks and valleys with an amplitude on the order of Φ_0 on the supercomputer. Further, when the magnetic field being applied is reduced while the sample passes through its transition temperature (9.2K for Nb) for cooling, we noted that the unevenness of the magnetic field distribution generated by the trapped flux quanta was reduced.

As described above, we developed a new system to detect trapped flux quanta using the detection coil of a SQUID fluxmeter to scan the surface of a supercomputer. This system has the following features: (1) It is capable of detecting the trapped flux by reducing the effect of the external magnetic disturbance; (2) it is applicable to simple supercomputers other than the Josephson junction; and (3) it is capable of detecting flux quanta over a superconductor with a sufficiently large area or a pot-like superconducting shield.

Sweeping of Trapped Flux in Superconductors Using Laser Beam Scanning

Qiquan Geng, Hirofumi Minami, Kazunori Chihara, Junpei Yuyama, and Eiichi Goto

A new technique has been developed to remove flux quanta trapped in superconducting film. It consists of measuring the magnetic field distribution over a superconductor with an rf-SQUID and removing the detected trapped flux using laser beam scanning. The trapped flux movement follows the motion of the Ar laser beam exactly. By scanning the laser beam over the trapped flux quanta, the trapped flux is successfully moved to any desired location.

Technique for Measuring Absolute Intensity of Weak Magnetic Fields by a SQUID Pick-up Coil System

Qiquan Geng, Hirofumi Minami, Kazunori Chihara, Junpei Yuyama, and Eiichi Goto

A method to measure the absolute intensity of a weak magnetic field is described. This method uses patterned superconducting strip lines as a spatial modulator of the field and detected the magnetic field distribution over them as a function of applied magnetic fields. The field distribution change measured by an rf-SQUID system is proportional to the component of the absolute intensity of the magnetic field at the specimen that is parallel with the pick-up coil axis. The magnetic field intensity can be determined absolutely from about 5 μG by this method. A spatial resolution of the field as good as a few millimeters is obtained. Some practical limitations of this method are also discussed.

Magnetic Field Distribution Arising From a Trapped Fluxon

Qiquan Geng, Kazunori Chihara, and Eiichi Goto

The primary purpose of this work is to develop a simple detection method to detect the location of a single vortex trapped in a Josephson junction or a superconducting groundplane. For this purpose, simple model calculations are performed in relation to the potential and the magnetic field distribution produced by a trapped fluxon in thin superconducting films to detect flux quantum by the SQUID pick-up coil. Comparison with experiments indicates that our model is potentially useful in the SQUID imaging process, though some deviations are seen.

Ultrahigh Vacuum Application of a Refrigerator-Cooled Cryopump

M. Kasuya and J. Yuyama

A computer that uses a superconducting device like the QFP requires a superconducting magnetic shield with little flux trapping. To this end, it is necessary to make uniform superconducting films with few impurities or defects in their crystals. To realize the ultrahigh vacuum required for such films, we manufactured an aluminum alloy, ultrahigh vacuum unit using a mechanical cryopump.

A stainless steel ultrahigh vacuum unit equipped with a conventional mechanical cryopump needed a bake-out of more than 250°C to obtain the required ultrahigh vacuum. This in turn necessitated a measure to prevent overheating by the refrigerator during the bake-out, which led to very poor operability.

The advantage of our ultrahigh vacuum unit featuring a mechanical cryopump is that the bake-out temperature is reduced to 120°C from 250°C by using an aluminum alloy for the component materials of the vacuum chamber and pump case. This makes it unnecessary to have an overheating prevention measure, as is required for the stainless steel exhaust units of conventional refrigerators.

Further, we conducted an experiment to determine if it is possible to obtain an ultrahigh vacuum without the bake-out, and if the attainable pressure will change when the processing method is changed before restarting the cryopump. The results of these studies clarified the following points:

(1) Without a special measure to prevent overheating, it is possible to bake out the vacuum chamber at about 120°C and to obtain a pressure of 4-5 x 10^{-9} Pa. That is, it is possible to have a bake-out without damaging the mechanical cryopump. This is because of the characteristics of the aluminum alloy, which can withstand a low-temperature bake-out.

(2) By supplying dry nitrogen directly from liquid nitrogen, using this gas, and setting back the vacuum chamber pressure to the atmospheric pressure, it is possible to prevent water from adhering to the vacuum chamber wall, thus making it possible to attain the necessary pressure of 4-5 x 10^{-9} Pa without the need of a bake-out.

Although the helium gas contained in the atmosphere is somewhat hard for a mechanical cryopump to handle, it is possible to minimize the helium gas partial pressure by supplying dry nitrogen gas rather than air, and the necessary pressure of 4-5 x 10^{-9} Pa can be attained easily.

(3) The cryopump is a reservoir type that needs to be reactivated after a certain operating time. Thus we examined the following three methods as ways to reactivate the cryopump used in an ultrahigh vacuum.

i) Simply raising the temperature of the cryopump to room temperature.

ii) Flushing the cryopump with dry nitrogen after raising its temperature to room temperature.

iii) Heating the cryopump from the external pump housing using a heater after raising its temperature (about 90°C at the baffle temperature).

We found that there is no significant difference among the three methods in terms of the attainable pressure after reactivation.

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